SEMICONDUCTOR

CD4021BC 8-Stage Static Shift Register

General Description

The CD4021BC is an 8-stage parallel input/serial output shift register. A parallel/serial control input enables individual JAM inputs to each of 8 stages. Q outputs are available from the sixth, seventh, and eighth stages. All outputs have equal source and sink current capabilities and conform to standard "B" series output drive.

When the parallel/serial control input is in the logical "0" state, data is serially shifted into the register synchronously with the positive transition of the clock. When the parallel/ serial control is in the logical "1" state, data is jammed into each stage of the register asynchronously with the clock.

All inputs are protected against static discharge with diodes to $\rm V_{DD}$ and $\rm V_{SS}.$

Features

■ Wide supply voltage range: 3.0V to 15V

- High noise immunity: 0.45 V_{DD} (typ.)
- Low power TTL compatibility:

Fan out of 2 driving 74L or 1 driving 74LS ■ 5V–10V–15V parametric ratings

Symmetrical output characteristics

Maximum input leakage 1 µA at 15V over full temperature range

Ordering Code:

Order Number	Order Code	Package Description
CD4021BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4021BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Truth Table

C _L (Note 1)	Serial Input	Parallel/ Serial Control	PI 1	PI n	Q1 (Internal)	Q _n (Note 2)		
Х	Х	1	0	0	0	0		
Х	х	1	0	1	0	1		
Х	Х	1	1	0	1	0		
Х	Х	1	1	1	1	1		
~	0	0	Х	Х	0	Q _{n-1}		
~	1	0	Х	Х	1	Q _{n-1}		
~	Х	0	Х	Х	Q1	Qn		

X = Don't care case Note 1: Level change

Note 2: No change

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Absolute Maximum Ratings(Note 3)

Recommended Operating Conditions (Note 4)

(Note 4)	
Supply Voltage (V _{DD})	-0.5V to +18V
Input Voltage (V _{IN})	–0.5V to V _{DD} +0.5V
Storage Temperature Range (T _S)	$-65^{\circ}C$ to $+150^{\circ}C$
Power Dissipation (P _D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T _L)	
(Soldering, 10 seconds)	260°C

Supply Voltage (V_{DD}) 3V to 15V 0 to V_{DD} Input Voltage (VIN) Operating Temperature Range (T_A) CD4021BCN

-55°C to +125°C

CD4021BC

Note 3: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guranteed. Except for "Operating Tempera-ture Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 4: V_{SS} = 0V unless otherwise specified.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	–55°C		+25°C			+125°C		Unite
		Conditions	Min	Max	Min	Тур	Max	Min	Max	Units
I _{DD}	Quiescent Device	$V_{DD} = 5V$, $V_{IN} = V_{DD}$ or V_{SS}		5		0.1	5		150	
	Current	$V_{DD} = 10V, V_{IN} = V_{DD} \text{ or } V_{SS}$		10		0.2	10		300	μΑ
		$V_{DD} = 15V$, $V_{IN} = V_{DD}$ or V_{SS}		20		0.3	20		600	
V _{OL}	LOW Level	$V_{DD} = 5V$		0.05		0	0.05		0.05	
	Output Voltage	$V_{DD} = 10V \qquad I_O < 1 \ \mu A$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	
V _{OH}	HIGH Level	$V_{DD} = 5V$	4.95		4.95	5		4.95		
	Output Voltage	$V_{DD} = 10V \qquad I_O < 1 \ \mu A$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		
VIL	LOW Level	$V_{DD} = 5V, V_{O} = 0.5V \text{ or } 4.5V$		1.5		2	1.5		1.5	
	Input Voltage	$V_{DD} = 10V, V_{O} = 1.0V \text{ or } 9.0V$		3.0		4	3.0		3.0	V
		$V_{DD} = 15V, V_{O} = 1.5V \text{ or } 13.5V$		4.0		6	4.0		4.0	
VIH	HIGH Level	$V_{DD} = 5V, V_{O} = 0.5V \text{ or } 4.5V$	3.5		3.5	3		3.5		
	Input Voltage	$V_{DD} = 10V, V_{O} = 1.0V \text{ or } 9.0V$	7.0		7.0	6		7.0		V
		$V_{DD} = 15V, V_{O} = 1.5V \text{ or } 13.5V$	11.0		11.0	9		11.0		
I _{OL}	LOW Level Output	$V_{DD} = 5V, V_{O} = 0.4V$	0.64		0.51	0.88		0.36		
	Current (Note 5)	$V_{DD} = 10V, V_{O} = 0.5V$	1.6		1.3	2.2		0.90		mA
		$V_{DD} = 15V, V_{O} = 1.5V$	4.2		3.4	8		2.4		
I _{OH}	HIGH Level Output	$V_{DD} = 5V, V_{O} = 4.6V$	-0.64		-0.51	-0.88		-0.36		
	Current (Note 5)	$V_{DD} = 10V, V_{O} = 9.5V$	-1.6		-1.3	-2.2		-0.90		mA
		$V_{DD} = 15V, V_{O} = 13.5V$	-4.2		-3.4	-8		-2.4		
I _{IN}	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		-0.1		-10 ⁻⁵	-0.1		-1.0	ıιΔ
		$V_{DD} = 15V, V_{IN} = 15V$		0.1		10 ⁻⁵	0.1		1.0	μΑ

Note 5: I_{OH} and I_{OL} are tested one output at a time.

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AC Electrical Characteristics (Note 6)

 ${\sf T}_{A}=25^{\circ}C,~input~t_{r},~t_{f}=20~ns,~C_{L}=50~pF,~R_{L}=200~{\sf k}\Omega$ Symbol Parameter Conditions Min Тур Max Units Propagation Delay Time $V_{DD} = 5V$ 240 350 t_{PLH}, t_{PHL} $V_{DD} = 10V$ 100 175 ns $V_{DD} = 15V$ 70 140 $V_{DD} = 5V$ Transition Time 100 200 $t_{THL},\,t_{TLH}$ $V_{DD} = 10V$ 50 100 ns $V_{DD} = 15V$ 40 80 Maximum Clock $V_{DD} = 5V$ 25 35 f_{CL} Input Frequency $V_{DD} = 10V$ 5 10 MHz $V_{DD} = 15V$ 8 16 Minimum Clock tw $V_{DD} = 5V$ 100 200 Pulse Width $V_{DD} = 10V$ 50 100 ns $V_{DD} = 15V$ 40 80 $V_{DD} = 5V$ t,CL, t,CL Clock Rise and 15 Fall Time (Note 6) $V_{DD} = 10V$ 15 μs $V_{DD} = 15V$ 15 Minimum Set-Up Time ts $V_{DD} = 5V$ 60 Serial Input 120 t_H ≥ 200 ns 40 80 $V_{DD} = 10V$ ns (Ref. to CL) $V_{DD} = 15V$ 30 60 Parallel Inputs $V_{DD} = 5V$ 25 50 t_H ≥ 200 ns $V_{DD} = 10V$ 15 30 ns $V_{DD} = 15V$ (Ref. to P/S) 10 20 $V_{DD} = 5V$ Minimum Hold Time 0 t_H Serial In, Parallel In, $t_s \ge 400 \text{ ns}$ $V_{DD} = 10V$ 10 ns Parallel/Serial Control $V_{DD} = 15V$ 15 $V_{DD} = 5V$ Minimum P/S 150 250 t_{WH} 75 Pulse Width $V_{DD} = 10V$ 125 ns $V_{DD} = 15V$ 50 100 Minimum P/S Removal $V_{DD} = 5V$ 100 200 t_{REM} $V_{DD} = 10V$ Time (Ref. to CL) 50 100 ns $V_{DD} = 15V$ 40 80 Average Input Capacitance CI Any Input 5 7.5 pF C_{PD} Power Dissipation 100 pF Capacitance (Note 8)

Note 6: AC Parameters are guaranteed by DC correlated testing.

Note 7: If more than one unit is cascaded t_rCL should be made less than or equal to the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

Note 8: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 74C family characteristics application note AN-90.



CD4021BC





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