

Instruments
Data sheet acquired from Harris Semiconductor SCHS061

CD4086B Types

CMOS Expandable 4-Wide 2-Input AND-OR-INVERT Gate

High-Voltage Types (20-Volt Rating)

CD4086B contains one 4-wide 2-input AND-OR-INVERT gate with an INHIBIT/EXP input and an ENABLE/EXP input. For a 4-wide A-O-I function INHIBIT/EXP is tied to V_{SS} and ENABLE/EXP to V_{DD}. See Fig.10 and its associated explanation for applications where a capability greater than 4-wide is required.

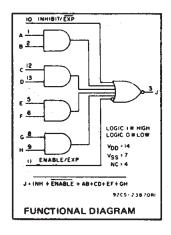
The CD4086B is supplied in 14-lead dual-inline ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

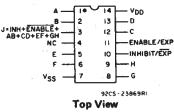
Features:

- Medium-speed operation tpHL = 90 ns; tpLH = 140 ns (typ.) at 10 V
- INHIBIT and ENABLE inputs
- Buffered outputs
- 100% tested for quiescent current at 20 V
- Maximum input leakage current of 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package termperature range):

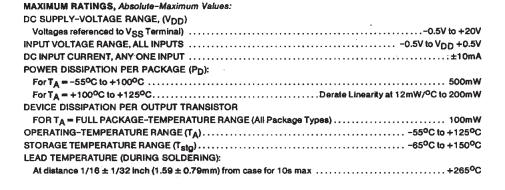
1 V at V_{DD} = 5 V 2 V at V_{DD} = 10 V 2.5 V at V_{DD} = 15 V

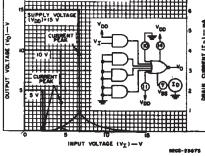
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"





TERMINAL ASSIGNMENT





AMBIENT TEMPERATURE (TA)-25°C

Fig. 1 — Typical voltage and current transfer characteristics.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

	LIN			
CHARACTERISTIC	MIN.	MAX.	UNITS	
Supply-Voltage Range (For T _A = Full Package- Temperature Range)	3	18	٧	

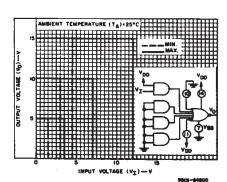


Fig. 2 — Minimum and maximum voltage transfer characteristics,

STATIC ELECTRICAL CHARACTERISTICS

CHARAC- TERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)						UNITS	
TENISTIC	· Vo	VIN	V _{DD}						+25		
	(V).	(V)	(V)	55	-40	+85	+125	Min.	Тур.	Max.	
Quiescent		0,5	5	1	1	30	30	<u>~</u>	0.02	1	
Device		0,10	10	2	2	60	60		0.02	2	
Current	_	0,15	15	4	4	120	120		0.02	4	μΑ
IDD Max.	_	0,20	20	20	20	600	600		0.04	20	()
Output Low								: 2			
(Sink)	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	3674 1	7.45 I	
Current,	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3°	2.6	_	
IOL Min.	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	_	
Output High	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	_	mA
(Source)	2.5	0,5	5	–2	-1.8	-1.3	-1,15	-1.6	-3.2		
Current,	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	_	
IOH Min.	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	-	
Output Volt-											
age:	_	0,5	5		0.0)5		_	0	0.05	
Low-Level,		0,10	10		0.0)5		-	0'	0.05	
V _{OL} Max.	. 7.a	0,15	15	0.05			-	0	0.05	v	
Output Volt-		8.44				· · · ·					V
age:	-	0,5	5		4.9	95		4.95	5	_	
High-Level,	_	0,10	10		9.9	95		9.95	10	_	
V _{OH} Min.	-	0,15	15		14.	95		14.95	15	-	
Input Low	0.5,4.5		5		1.	5		_	_	1.5	
Voltage,	1,9	-	10		3			_	_	3	
VIL Max.	1.5,13.5	_	15		4				_	4	.,
Input High	0.5,4.5	_	5		3.	5		3.5	_	_	٧
Voltage,	1,9	± :	10		7			7	_	_	
VIH Min.	1.5,13.5	-	15		1	1		11	_		
Input Current, I _{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	_	±10 ⁻⁵	±0.1	μΑ

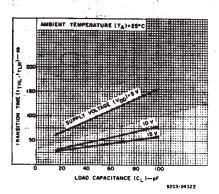


Fig.6 - Typical transition time vs. load capacitance.

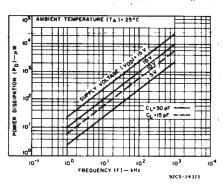


Fig.7 - Typical power dissipation vs. frequency.

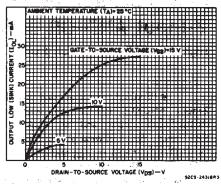


Fig. 3 — Typical output low (sink) current characteristics.

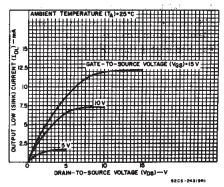


Fig. 4 — Minimum output low (sink) current characteristics.

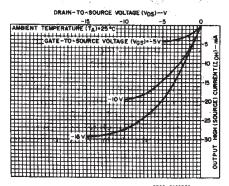


Fig.5 - Typical output high (source) current characteristics.

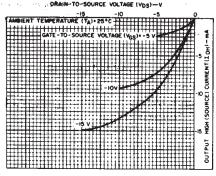
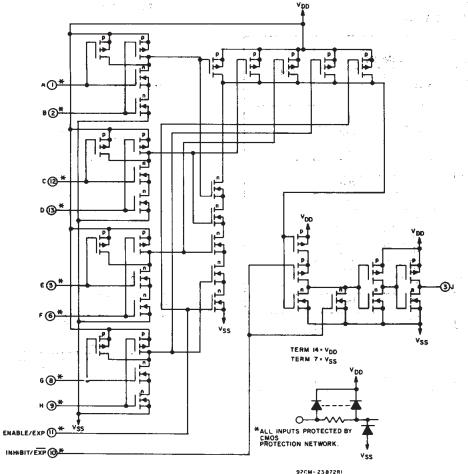


Fig.8 – Minimum output high (source) current characteristics.



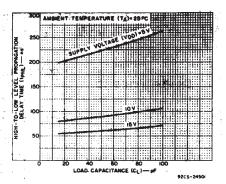


Fig. 11 — Typical DATA or ENABLE high-to-low level propagation delay time vs. load capacitance.

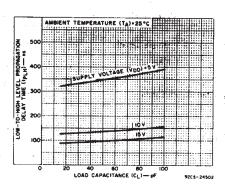
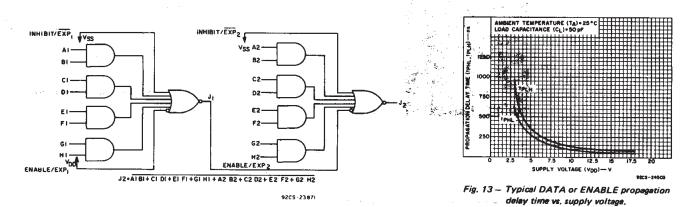


Fig. 12 — Typical DATA or ENABLE low-to-high level propagation delay time vs. load capacitance.

Fig. 9 - CD4086B schematic diagram.



CD4086B Types

Fig. 10 - Two CD40868's connected as an 8-wide 2-input A-O-I gate.

Fig. 10 above shows two CD4086's utilized to obtain an 8-wide 2-input A-O-I function. The output (J1) of one CD4086 is fed directly to the ENABLE/EXP2 line of the second CD4086. In a similar fashion, any

NAND gate output can be fed directly into the ENABLE/EXP input to obtain a 5-wide A-O-I function. In addition, any AND gate output can be fed directly into the IN-HIBIT/EXP input with the same result.

CD4086B Types

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C; Input t_r , t_f = 20 ns, C_L = 50 pF, R_L = 200 $k\Omega$

CHARACTERISTIC	CONDITIONS		LIN		
		V _{DD} (V)	TYP.	MAX.	UNITS
Propagation Delay Time (Data): High-to-Low Level, tpHL		5	225	450	
		10	90	180	ns
		15	60	120	1
Low-to-High Level, t _{PLH}		5	310	620	
		10	125	250	ns
	<u>L</u>	15	90	180	
Propagation Delay Time (Inhibit): High-to-Low Level, tpHL(INH)		5	150	300	
		10	60	120	ns
		15	40	80	1
Low-to-High Level, tPLH(INH)		5	250	500	
		10	100	200	ns
		15	70	140	
Transition Time, ^t THL ^{, t} TLH		5	100	200	
		10	50	100	ns
		15	40	80	7
Input Capacitance CIN	Any Input		5	7.5	pF

TEST CIRCUITS

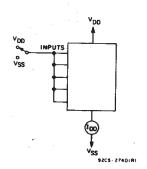


Fig. 14 - Quiescent device current.

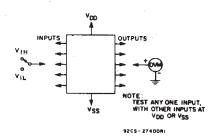
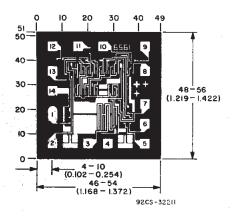


Fig. 15 - Input voltage.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3}) inch).

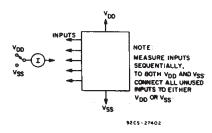


Fig. 16 - Input leakage current.

Dimensions and Pad Layout for the CD4086BH

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