

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4094B

MSI

8-stage shift-and-store bus register

Product specification
File under Integrated Circuits, IC04

January 1995

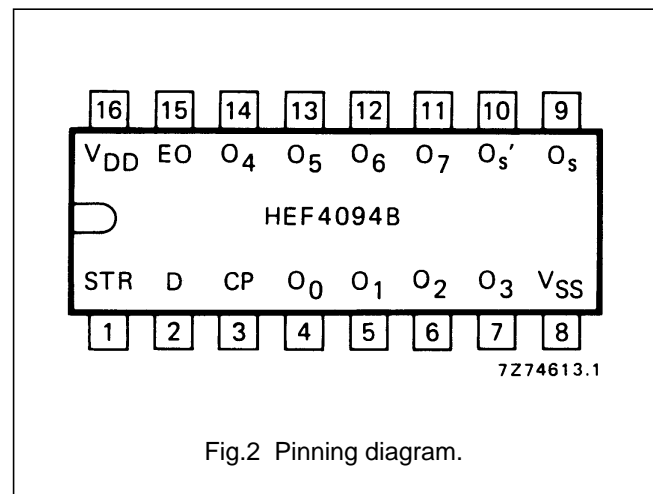
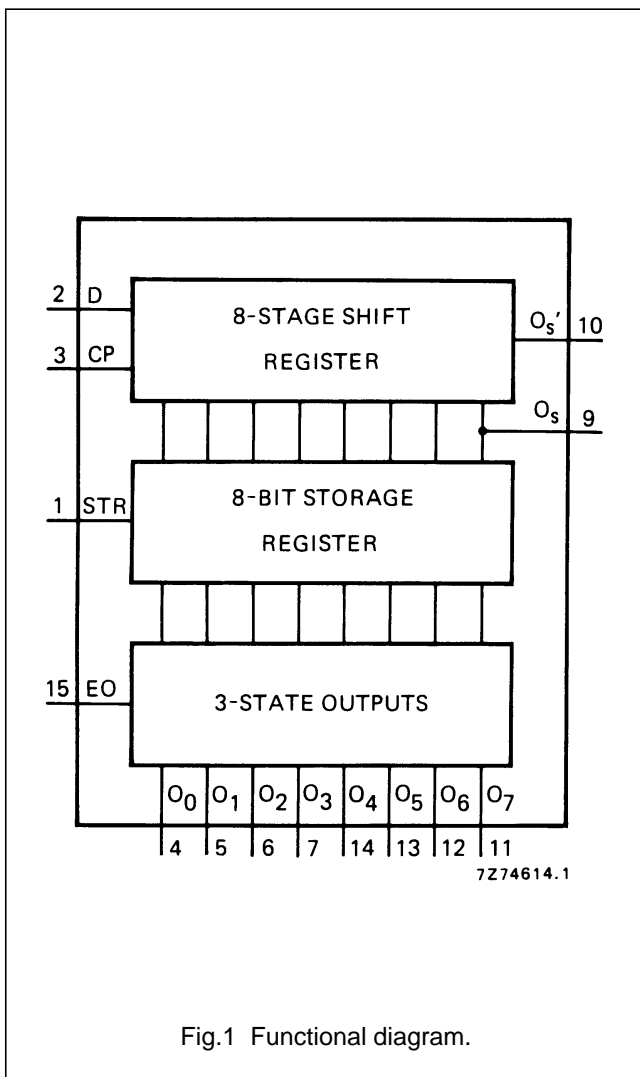
8-stage shift-and-store bus register

HEF4094B MSI

DESCRIPTION

The HEF4094B is an 8-stage serial shift register having a storage latch associated with each stage for strobing data from the serial input to parallel buffered 3-state outputs O_0 to O_7 . The parallel outputs may be connected directly to common bus lines. Data is shifted on positive-going clock transitions. The data in each shift register stage is transferred to the storage register when the strobe (STR) input is HIGH. Data in the storage register appears at the outputs whenever the output enable (EO) signal is HIGH.

Two serial outputs (O_s and O'_s) are available for cascading a number of HEF4094B devices. Data is available at O_s on positive-going clock edges to allow high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information is available at O'_s on the next negative-going clock edge and provides cascading HEF4094B devices when the clock rise time is slow.



- HEF4094BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4094BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4094BT(D): 16-lead SO; plastic (SOT109-1)
- (): Package Designator North America

PINNING

D	data input	EO	output enable input
CP	clock input	O_s, O'_s	serial outputs
STR	strobe input	O_0 to O_7	parallel outputs

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

8-stage shift-and-store bus register

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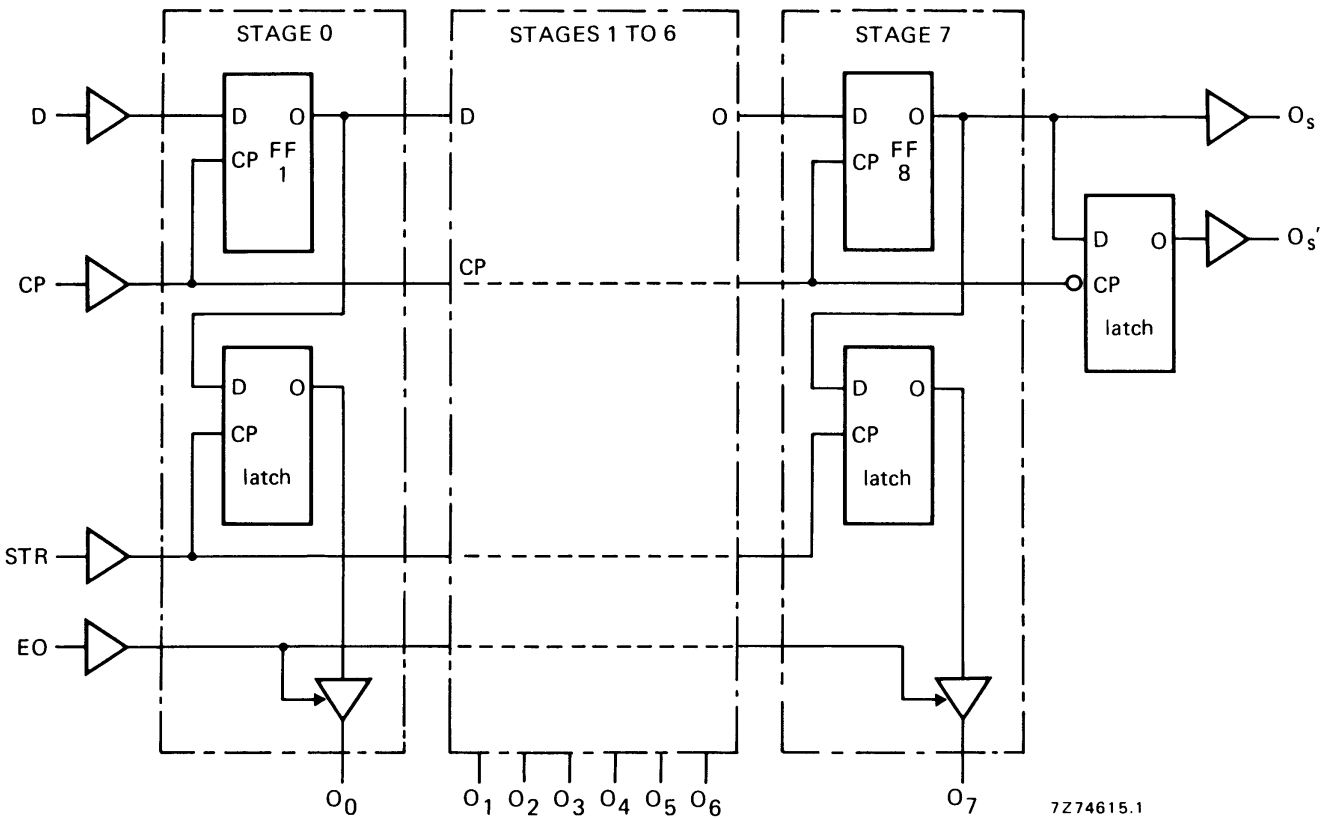


Fig.3 Logic diagram.

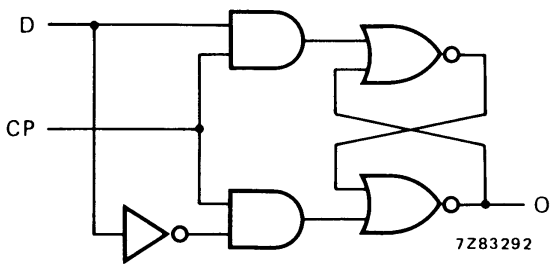


Fig.4 One D-latch.

8-stage shift-and-store bus register

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FUNCTION TABLE

INPUTS				PARALLEL OUTPUTS		SERIAL OUTPUTS	
CP	EO	STR	D	O ₀	O _n	O _s	O' _s
↗	L	X	X	Z	Z	O' ₆	nc
↘	L	X	X	Z	Z	nc	O ₇
↗	H	L	X	nc	nc	O' ₆	nc
↗	H	H	L	L	O _{n-1}	O' ₆	nc
↗	H	H	H	H	O _{n-1}	O' ₆	nc
↘	H	H	H	nc	nc	nc	O ₇

Notes

1. H = HIGH state (the more positive voltage)
2. L = LOW state (the less positive voltage)
3. X = state is immaterial
4. ↗ = positive-going transition
5. ↘ = negative-going transition
6. Z = high impedance off state
7. nc = no change
8. O'₆ = the information in the seventh shift register stage

At the positive clock edge the information in the 7th register stage is transferred to the 8th register stage and the O_s output.

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V _{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5 10 15	2100 f _i + ∑ (f _o C _L) × V _{DD} ² 9700 f _i + ∑ (f _o C _L) × V _{DD} ² 26 000 f _i + ∑ (f _o C _L) × V _{DD} ²	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) ∑ (f _o C _L) = sum of outputs V _{DD} = supply voltage (V)

8-stage shift-and-store bus register

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MSI**AC CHARACTERISTICS** $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ °C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	SYMBOL	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA					
Propagation delays	5	t_{PHL}	135	270	ns	108 ns + (0,55 ns/pF) C_L					
							HIGH to LOW	65	130	ns	54 ns + (0,23 ns/pF) C_L
	5	t_{PLH}	105	210	ns	78 ns + (0,55 ns/pF) C_L					
							LOW to HIGH	50	100	ns	39 ns + (0,23 ns/pF) C_L
	15	t_{PHL}	105	210	ns	78 ns + (0,55 ns/pF) C_L					
							HIGH to LOW	50	100	ns	39 ns + (0,23 ns/pF) C_L
	5	t_{PLH}	105	210	ns	78 ns + (0,55 ns/pF) C_L					
							LOW to HIGH	50	100	ns	39 ns + (0,23 ns/pF) C_L
	5	t_{PHL}	165	330	ns	138 ns + (0,55 ns/pF) C_L					
							HIGH to LOW	75	150	ns	64 ns + (0,23 ns/pF) C_L
	5	t_{PLH}	150	300	ns	123 ns + (0,55 ns/pF) C_L					
							LOW to HIGH	70	140	ns	59 ns + (0,23 ns/pF) C_L
5	t_{PHL}	110	220	ns	83 ns + (0,55 ns/pF) C_L						
						HIGH to LOW	50	100	ns	39 ns + (0,23 ns/pF) C_L	
											10
5	t_{PLH}	100	200	ns	73 ns + (0,55 ns/pF) C_L						
						LOW to HIGH	45	90	ns	34 ns + (0,23 ns/pF) C_L	
											10
5	t_{THL}	60	120	ns	10 ns + (1,0 ns/pF) C_L						
						HIGH to LOW	30	60	ns	9 ns + (0,42 ns/pF) C_L	
											10
5	t_{TLH}	60	120	ns	10 ns + (1,0 ns/pF) C_L						
						LOW to HIGH	30	60	ns	9 ns + (0,42 ns/pF) C_L	
											10
15	20	40	ns	6 ns + (0,28 ns/pF) C_L							

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	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	
3-state propagation delays						
Output enable times	5			40	80	ns
EO \rightarrow O _n	10	t _{PZH}		25	50	ns
HIGH	15			20	40	ns
LOW	5			40	80	ns
	10	t _{PZL}		25	50	ns
	15			20	40	ns
Output disable times	5			75	150	ns
EO \rightarrow O _n	10	t _{PHZ}		40	80	ns
HIGH	15			30	60	ns
LOW	5			80	160	ns
	10	t _{PLZ}		40	80	ns
	15			30	60	ns
Minimum clock pulse width	5		60	30		ns
LOW	10	t _{WCPL}	30	15		ns
	15		24	12		ns
Minimum strobe pulse width	5		40	20		ns
HIGH	10	t _{WSTRH}	30	15		ns
	15		24	12		ns
Set-up times	5		60	30		ns
D \rightarrow CP	10	t _{su}	20	10		ns
	15		15	5		ns
Hold times	5		5	-15		ns
D \rightarrow CP	10	t _{hold}	20	5		ns
	15		20	5		ns
Maximum clock pulse frequency	5		5	10		MHz
	10	f _{max}	11	22		MHz
	15		14	28		MHz

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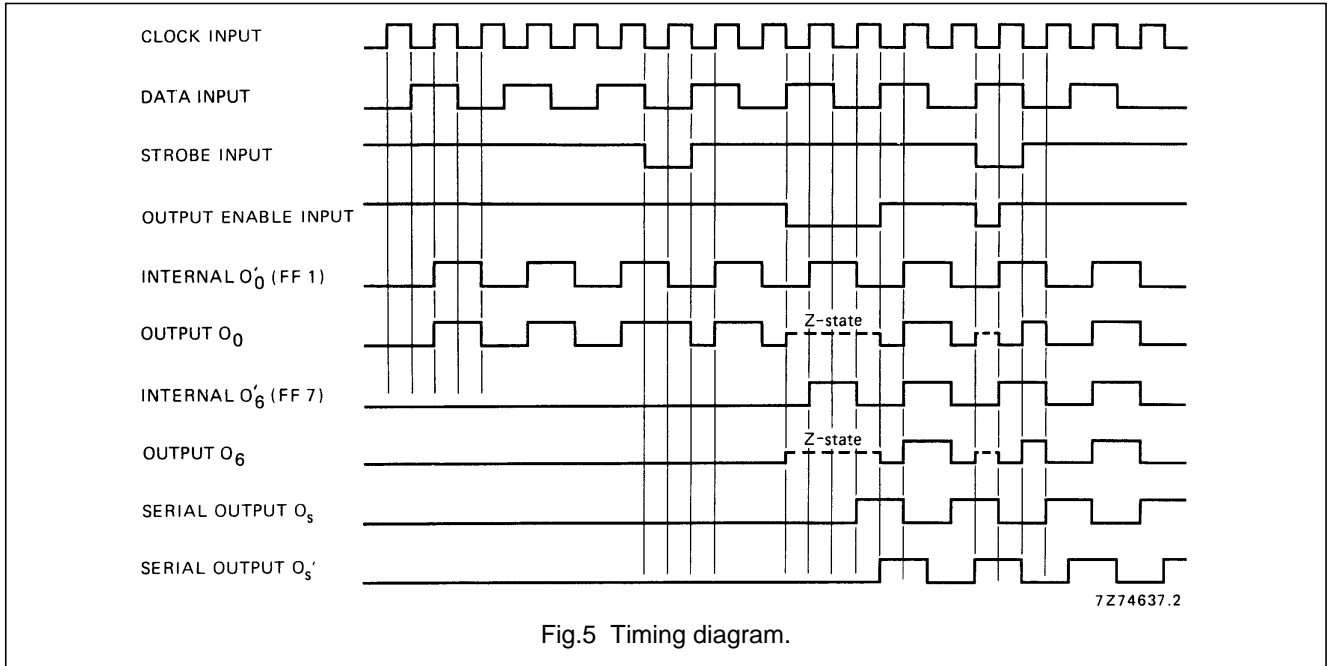


Fig.5 Timing diagram.

APPLICATION INFORMATION

Some examples of applications for the HEF4094B are:

- Serial-to-parallel data conversion
- Remote control holding register

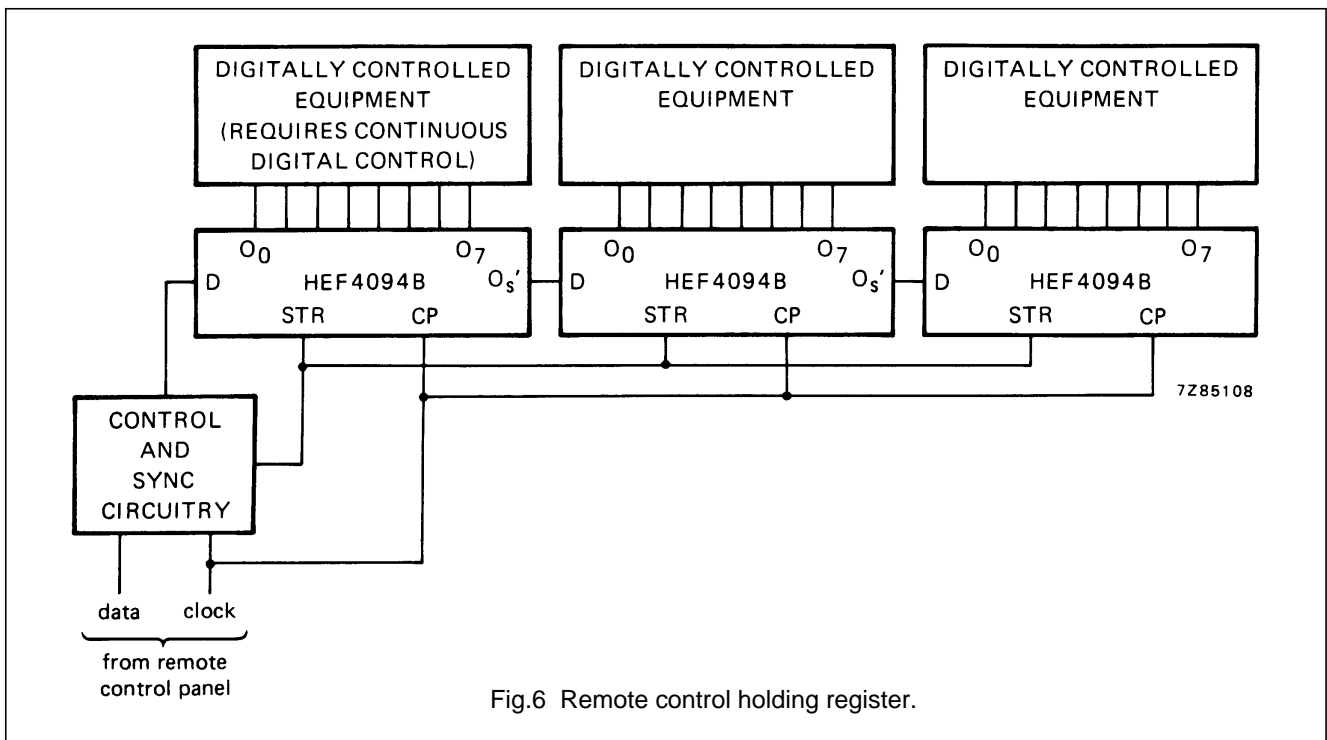


Fig.6 Remote control holding register.