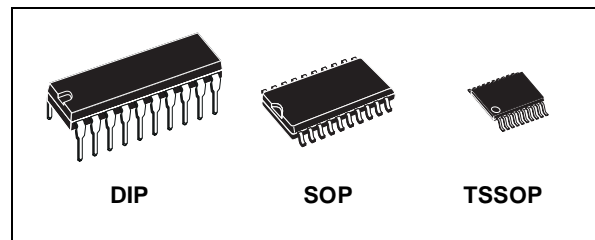


## OCTAL D-TYPE FLIP FLOP WITH CLEAR

- HIGH SPEED:
- $f_{MAX} = 250\text{MHz}$  (TYP.) at  $V_{CC} = 5\text{V}$
- LOW POWER DISSIPATION:  
 $I_{CC} = 8\mu\text{A}$ (MAX.) at  $T_A = 25^\circ\text{C}$
- HIGH NOISE IMMUNITY:  
 $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (MIN.)
- 50Ω TRANSMISSION LINE DRIVING CAPABILITY
- SYMMETRICAL OUTPUT IMPEDANCE:  
 $|I_{OH}| = I_{OL} = 24\text{mA}$  (MIN)
- BALANCED PROPAGATION DELAYS:  
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:  
 $V_{CC}$  (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 273
- IMPROVED LATCH-UP IMMUNITY



### ORDER CODES

PACKAGE	TUBE	T & R
DIP	74AC273B	
SOP	74AC273M	74AC273MTR
TSSOP		74AC273TTR

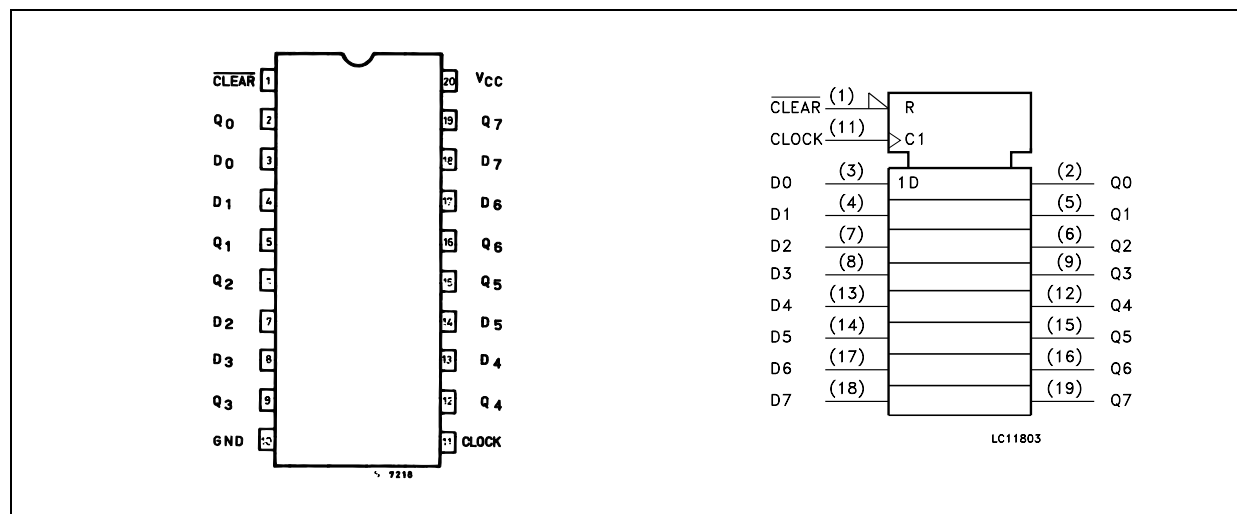
### DESCRIPTION

The 74AC273 is an advanced high-speed CMOS OCTAL D-TYPE FLIP FLOP WITH CLEAR fabricated with sub-micron silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology. Information signals applied to D inputs are

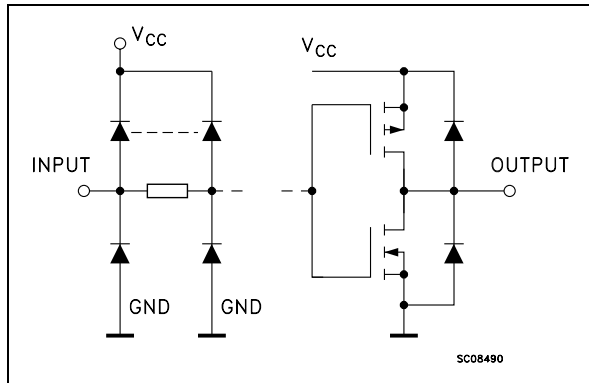
transferred to the Q output on the positive going edge of the clock pulse.

When the CLEAR input is held low, the Q outputs are held low independently of the other inputs. All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

### PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

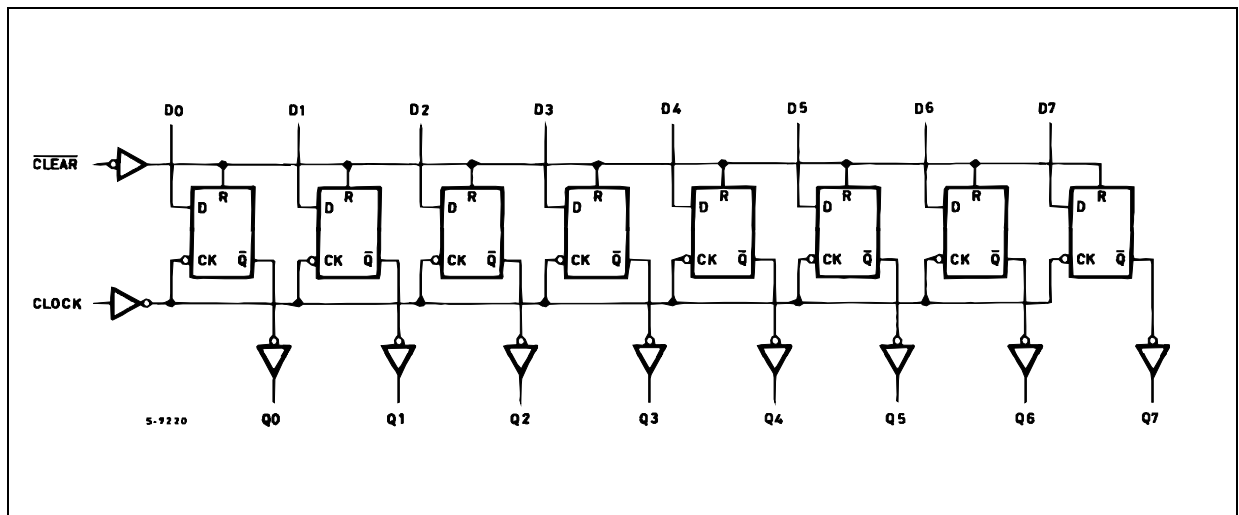
PIN No	SYMBOL	NAME AND FUNCTION
1	CLEAR	Asynchronous Master Reset (Active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q0 to Q7	Flip-Flop Outputs
3, 4, 7, 8, 13, 14, 17, 18	D0 to D7	Data Inputs
11	CLOCK	Clock Input (LOW-to-HIGH Edge Triggered)
10	GND	Ground (0V)
20	V <sub>CC</sub>	Positive Supply Voltage

TRUTH TABLE

INPUTS			OUTPUT	FUNCTION
$\overline{\text{CLEAR}}$	D	CLOCK	Q	
L	X	X	L	CLEAR
H	L		L	
H	H		H	
H	X		Q <sub>n</sub>	NO CHANGE

X : Don't Care

LOGIC DIAGRAM



This logic diagram has not been used to estimate propagation delays

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	-0.5 to +7	V
$V_I$	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
$V_O$	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	DC Input Diode Current	$\pm 20$	mA
$I_{OK}$	DC Output Diode Current	$\pm 20$	mA
$I_O$	DC Output Current	$\pm 50$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current	$\pm 400$	mA
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	2 to 6	V
$V_I$	Input Voltage	0 to $V_{CC}$	V
$V_O$	Output Voltage	0 to $V_{CC}$	V
$T_{op}$	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time $V_{CC} = 3.0, 4.5$ or $5.5V$ (note 1)	8	ns/V

1)  $V_{IN}$  from 30% to 70% of  $V_{CC}$

## DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V <sub>IH</sub>	High Level Input Voltage	3.0	V <sub>O</sub> = 0.1 V or V <sub>CC</sub> -0.1V	2.1	1.5		2.1		2.1		V
		4.5		3.15	2.25		3.15		3.15		
		5.5		3.85	2.75		3.85		3.85		
V <sub>IL</sub>	Low Level Input Voltage	3.0	V <sub>O</sub> = 0.1 V or V <sub>CC</sub> -0.1V		1.5	0.9		0.9		0.9	V
		4.5			2.25	1.35		1.35		1.35	
		5.5			2.75	1.65		1.65		1.65	
V <sub>OH</sub>	High Level Output Voltage	3.0	I <sub>O</sub> =-50 μA	2.9	2.99		2.9		2.9		V
		4.5	I <sub>O</sub> =-50 μA	4.4	4.49		4.4		4.4		
		5.5	I <sub>O</sub> =-50 μA	5.4	5.49		5.4		5.4		
		3.0	I <sub>O</sub> =-12 mA	2.56			2.46		2.4		
		4.5	I <sub>O</sub> =-24 mA	3.86			3.76		3.7		
		5.5	I <sub>O</sub> =-24 mA	4.86			4.76		4.7		
V <sub>OL</sub>	Low Level Output Voltage	3.0	I <sub>O</sub> =50 μA		0.002	0.1		0.1		0.1	V
		4.5	I <sub>O</sub> =50 μA		0.001	0.1		0.1		0.1	
		5.5	I <sub>O</sub> =50 μA		0.001	0.1		0.1		0.1	
		3.0	I <sub>O</sub> =12 mA			0.36		0.44		0.5	
		4.5	I <sub>O</sub> =24 mA			0.36		0.44		0.5	
		5.5	I <sub>O</sub> =24 mA			0.36		0.44		0.5	
I <sub>I</sub>	Input Leakage Current	5.5	V <sub>I</sub> = V <sub>CC</sub> or GND			± 0.1		± 1		± 1	μA
I <sub>CC</sub>	Quiescent Supply Current	5.5	V <sub>I</sub> = V <sub>CC</sub> or GND			8		80		160	μA
I <sub>OLD</sub>	Dynamic Output Current (note 1, 2)	5.5	V <sub>OLD</sub> = 1.65 V max					75		50	mA
I <sub>OHD</sub>			V <sub>OHD</sub> = 3.85 V min					-75		-50	mA

1) Maximum test duration 2ms, one output loaded at time

2) Incident wave switching is guaranteed on transmission lines with impedances as low as 50Ω

**AC ELECTRICAL CHARACTERISTICS** ( $C_L = 50 \text{ pF}$ ,  $R_L = 500 \Omega$ , Input  $t_r = t_f = 3\text{ns}$ )

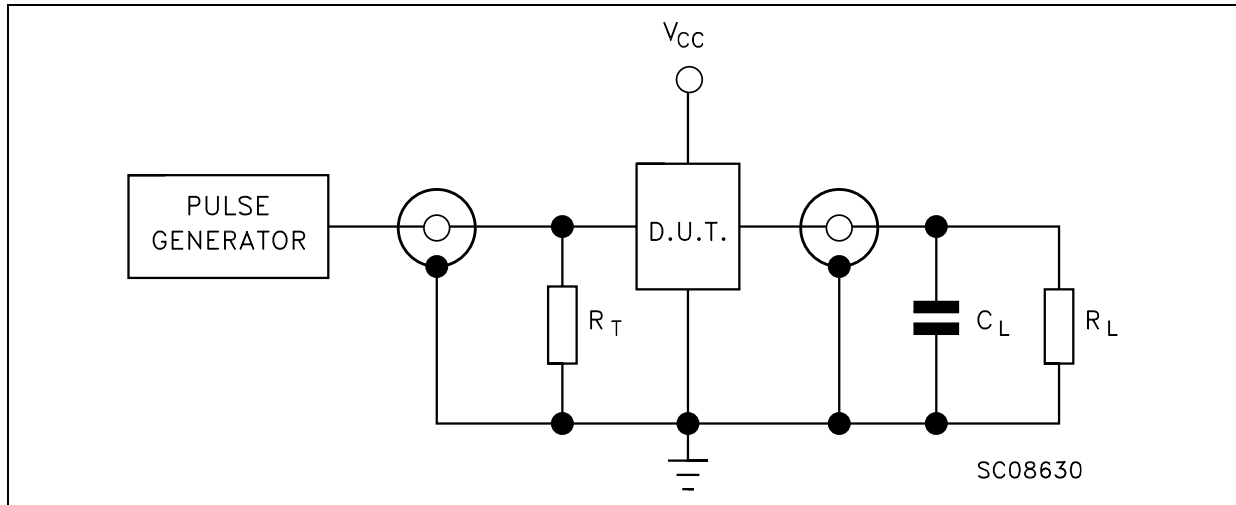
Symbol	Parameter	Test Condition		Value						Unit	
		$V_{CC}$ (V)		$T_A = 25^\circ\text{C}$			$-40 \text{ to } 85^\circ\text{C}$		$-55 \text{ to } 125^\circ\text{C}$		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time CLOCK to Q	3.3(*)		4.0	7.5	12.5	3.0	14.0	3.0	16.0	ns
		5.0(**)		3.0	5.0	9.0	2.5	10.0	2.5	11.0	
$t_{PHL}$	Propagation Delay Time CLEAR to Q	3.3(*)		4.0	8.5	13.0	3.0	14.0	3.0	16.0	ns
		5.0(**)		3.0	6.5	10.0	2.5	11.0	2.5	12.0	
$t_W$	CLEAR Pulse Width, LOW	3.3(*)		5.5			6.0		6.0		ns
		5.0(**)		4.0			4.5		4.5		
$t_W$	CLOCK Pulse Width	3.3(*)		5.5			6.0		6.0		ns
		5.0(**)		4.0			4.5		4.5		
$t_s$	Setup Time D to CLOCK, HIGH or LOW	3.3(*)		5.5			6.0		6.0		ns
		5.0(**)		4.0			4.5		4.5		
$t_h$	Hold Time D to CLOCK, HIGH or LOW	3.3(*)		1.5			1.5		1.5		ns
		5.0(**)		1.5			1.5		1.5		
$t_{REM}$	Recovery Time CLEAR to CLOCK	3.3(*)		4.0			4.5		4.5		ns
		5.0(**)		3.0			3.0		3.0		
$f_{MAX}$	Maximum Clock Frequency	3.3(*)		90			75		75		MHz
		5.0(**)		140	250		125		125		

(\*) Voltage range is  $3.3\text{V} \pm 0.3\text{V}$ (\*\*) Voltage range is  $5.0\text{V} \pm 0.5\text{V}$ 
**CAPACITIVE CHARACTERISTICS**

Symbol	Parameter	Test Condition		Value						Unit	
		$V_{CC}$ (V)		$T_A = 25^\circ\text{C}$			$-40 \text{ to } 85^\circ\text{C}$		$-55 \text{ to } 125^\circ\text{C}$		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
$C_{IN}$	Input Capacitance	5.0			4						pF
$C_{PD}$	Power Dissipation Capacitance (note 1)	5.0	$f_{IN} = 10\text{MHz}$		32						pF

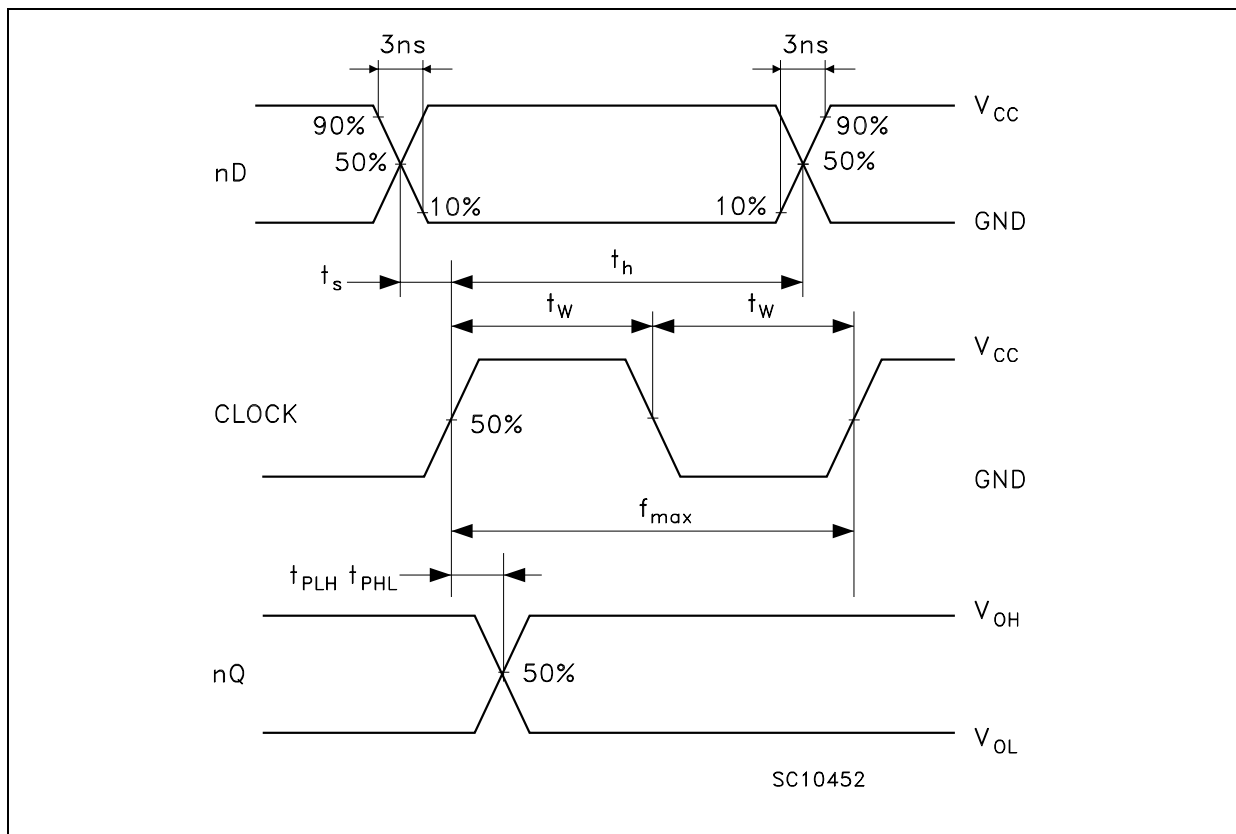
1)  $C_{PD}$  is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation.  $I_{CC(OP)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8$  (per circuit)

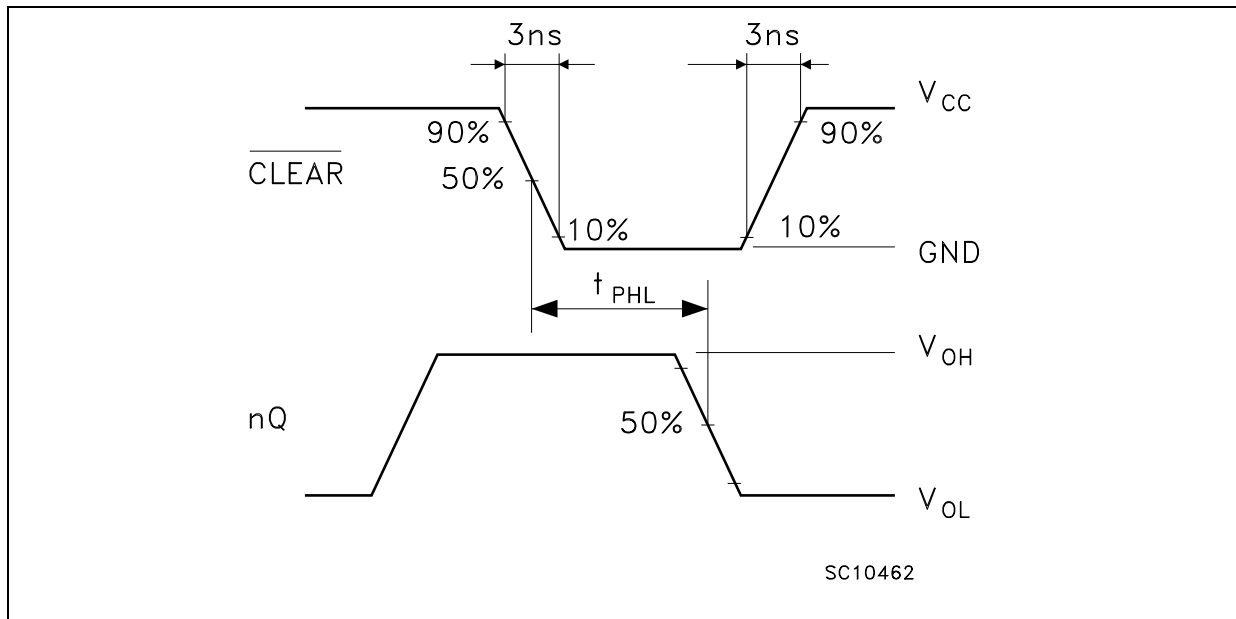
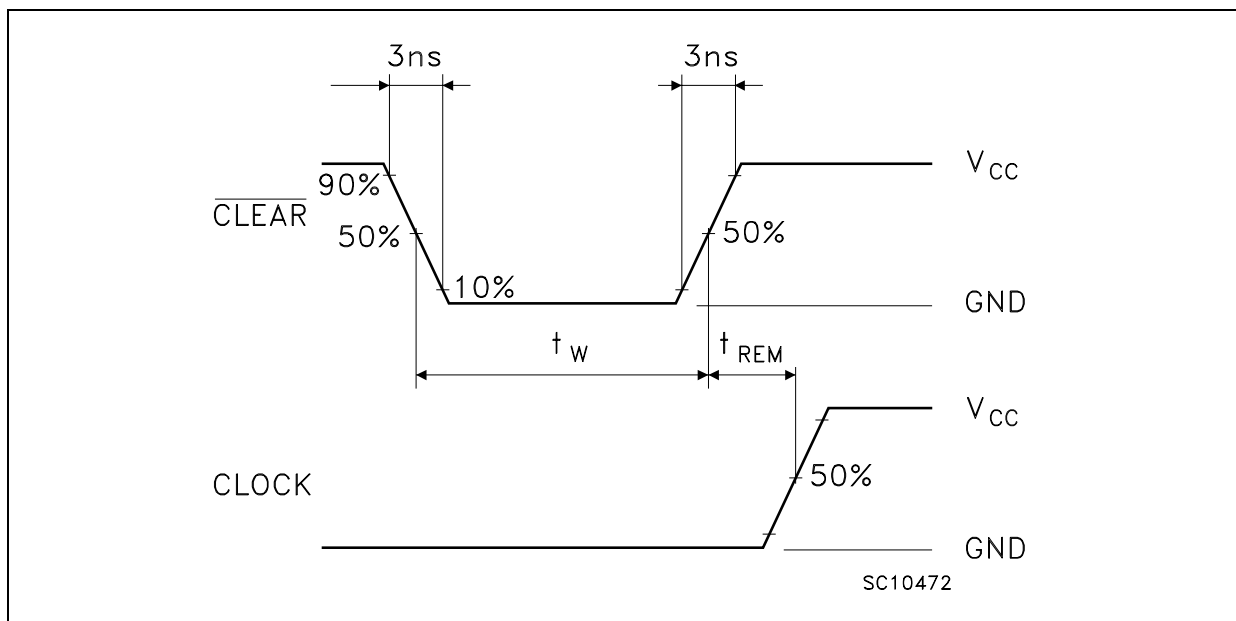
TEST CIRCUIT



$C_L = 50\text{pF}$  or equivalent (includes jig and probe capacitance)  
 $R_L = R_1 = 500\Omega$  or equivalent  
 $R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

WAVEFORM 1: PROPAGATION DELAYS, SETUP AND HOLD TIMES ( $f=1\text{MHz}$ ; 50% duty cycle)



**WAVEFORM 2: PROPAGATION DELAYS** ( $f=1\text{MHz}$ ; 50% duty cycle)**WAVEFORM 3: RECOVERY TIME** ( $f=1\text{MHz}$ ; 50% duty cycle)

### Plastic DIP-20 (0.25) MECHANICAL DATA

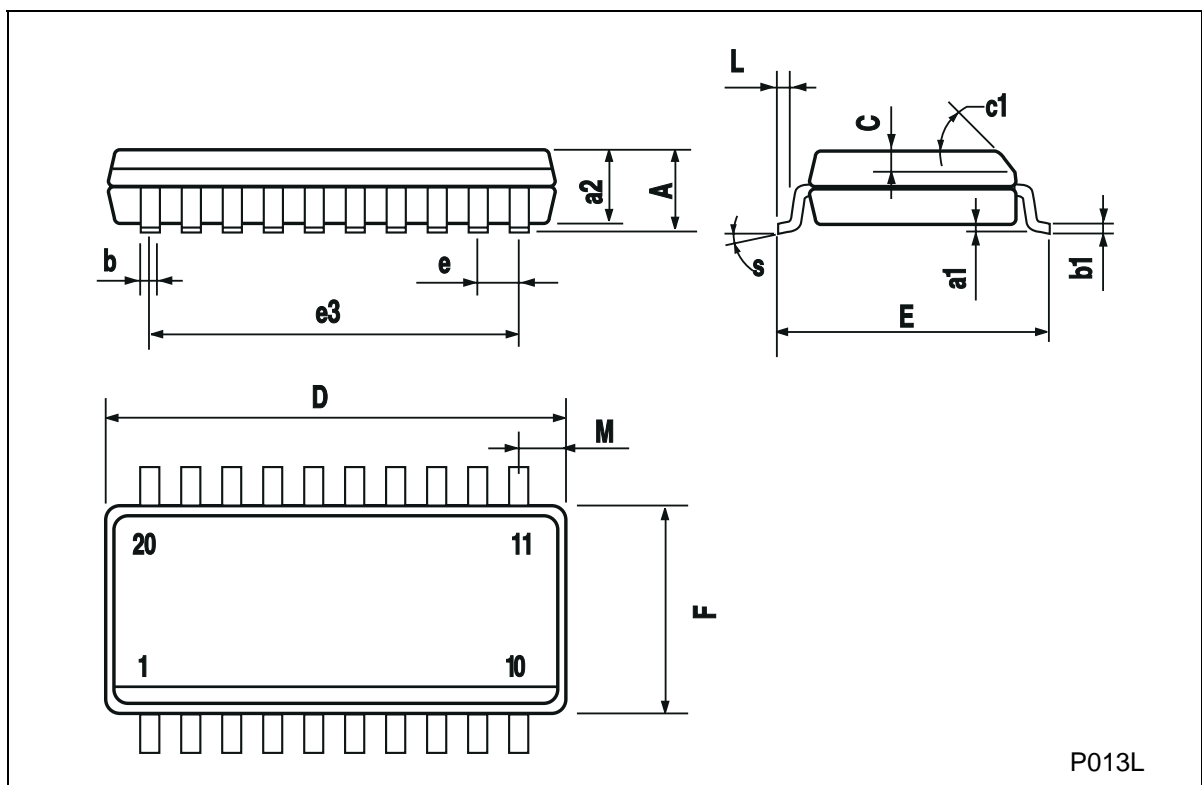
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053





## SO-20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.10		0.20	0.004		0.007
a2			2.45			0.096
b	0.35		0.49	0.013		0.019
b1	0.23		0.32	0.009		0.012
C		0.50			0.020	
c1	45 (typ.)					
D	12.60		13.00	0.496		0.512
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.40		7.60	0.291		0.299
L	0.50		1.27	0.19		0.050
M			0.75			0.029
S	8 (max.)					



## TSSOP20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.433
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.85	0.9	0.95	0.335	0.354	0.374
b	0.19		0.30	0.0075		0.0118
c	0.09		0.2	0.0035		0.0079
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.25	6.4	6.5	0.246	0.252	0.256
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°	4°	8°	0°	4°	8°
L	0.50	0.60	0.70	0.020	0.024	0.028



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