16650 UART – Universal Asynchronous Receiver/Transmitter
- with FIFOs

RealFast Intellectual Property

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Features

- Available under terms of the SignOnce IP License

- Follows the standard UART 16550 specification

- In FIFO mode, the transmitter and receiver are each buffered with 16-byte FIFOs to reduce the number of interrupts presented to the CPU

- Adds or deletes standard asynchronous communication bits (start, stop and parity) to or from the serial data

- Programmable baud generator divides any input clock by 1 to (216 - 1) and generates the 16 x clock

- Modem control functions (CTS, RTS, DSR, DTR, RI, and DCD)

- Fully configurable registers through a 8 bit interface

Applications

The core is suitable for implementing serial interfaces in a wide range of applications, including:

CORE Facts

Provided with Core	
Documentation	Core documentation
Design File Formats	EDIF netlist; VHDL Source RTL (available at extra cost)
Constraints Files	16550_uart.ucf
Verification	VHDL test bench
Instantiation templates	VHDL
Reference designs & application notes	None
Additional Items	None
Simulation Tool Used	
Modelsim v6.0	
Support	
Support provided by [RealFast AB]	

- Serial communication with a computer

- Serial interface to some other hardware device

General Description

The 16550 core is a standard UART providing 100% compatibility with the Texas Instruments 16550 device. It performs serial-to-parallel conversion and vice versa. The data width is 8 bits. The 16550 can be run in either 16550-compatible character mode or in 16550-compatible FIFO mode, in which an internal FIFO relieves the CPU of excessive software overhead. Developed for easy reuse in Xilinx FPGA applications, the 16550 is available optimized for several device families with competitive utilization and performance characteristics.

Family	Example Device	Fmax (MHz)	Slices	IOB	GCLK
Spartan-IIE	XC2S50E-6	106	344	38	1
Virtex-II	XC2V80-6	97	349	38	1
Virtex-II Pro	XC2VP2-6	105	344	38	1

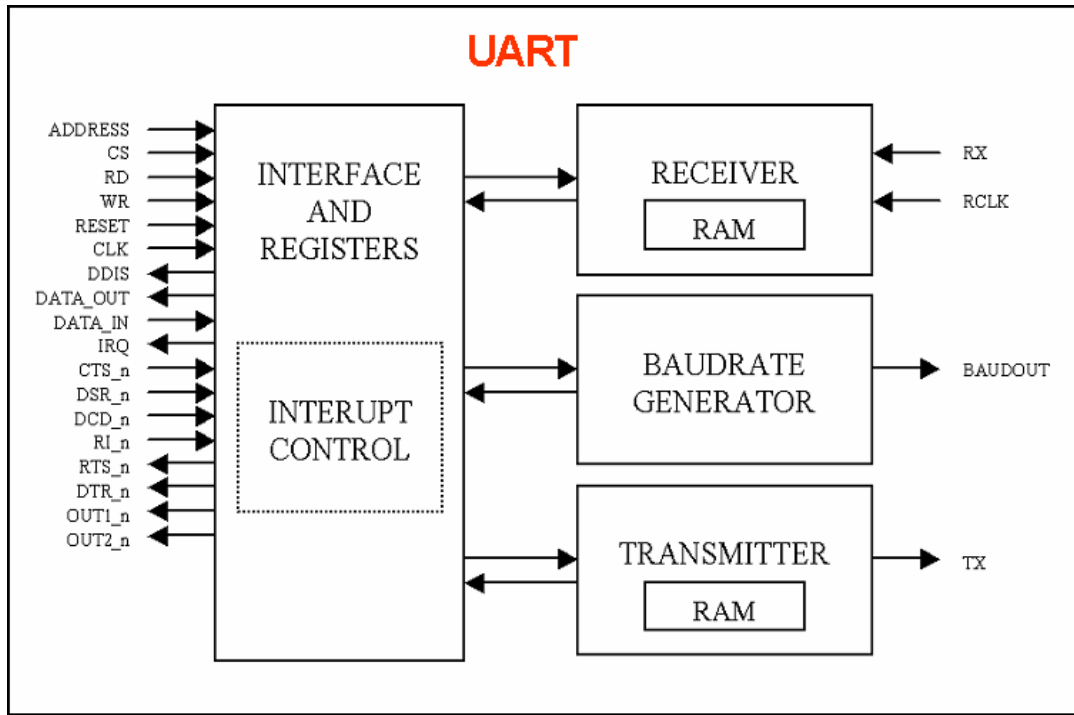**Table 1: Example Implementation Statistics**

Figure 1: The 16550 UART Core

Functional Description

As shown above and explained below, the 16550 includes four major blocks: Receiver, Transmitter, Interface / Registers and Baud Rate Generator.

Interface and registers

This block handles the communications with the application and it also contains all internal registers. All writing and reading of internal registers is accomplished through this block. The core uses two 8 bit wide databuses, one for read and one for write

The block also handles the interrupt control. It sends an interrupt signal to the application, depending on the state of the FIFO:s and its received and transmitted data. Various levels of interrupt can be read from the Interrupt Identification register, which gives the level of interrupt. Interrupts are sent in response to the condition of empty transmission or receiving buffers (or FIFOs), an error in the receiving of a character, or other conditions requiring the attention of the processor.

Receiver

The receiver block receives the incoming serial word and converts it to a 1 byte word if it is correct. The block is programmable to recognize data widths such as 5, 6, 7 or 8 bits, various parity settings such as even, odd, or no parity, and different stop bits: 1, 1½ and 2 bits. It checks for errors in the input data stream such as overrun errors, frame errors, parity errors and break errors. The incoming frame is either stored in the Receiver Holding register or in the Receiver FIFO, depending on the mode programmed.

Baud Rate Generator

This block takes the input clock, CLK, and divides it by a programmed value (from 1 to $2^{16} - 1$) to generate the reference baud clock. This clock can be connected to the input clock (RCLK) to provide a proper clock to the receiver. The baud clock is divided by 16 to create the transmission clock.

TXBlock

The Transmit block handles the transmission of data written to the Transmission Holding register (or transmit FIFO).

It adds required start, parity, and stop bits to the data being transmitted so that the receiving device can do the proper error handling and receiving.

Core Modifications

The size of the FIFOs can be changed. They can also be excluded. New registers can be added or existing ones can be deleted.

UART 16550 I/O Signals

The signal names of the 16550 core are shown in Table 2.

Signal	Direction	Description
RESET	Input	Master Reset (Asynchronous)
CLK	Input	Master clock
RCLK	Input	Receiver clock
RD	Input	Read control
WR	Input	Write control
CS	Input	Chip Select
DATAIN[7:0]	Input	Data Input Bus
CTS_n	Input	Clear to Send
DSR_n	Input	Data Set Ready
DCD_n	Input	Data Carrier Detect
RX	Input	Serial Input Data
RI_n	Input	Ring Indicator
ADDRESS[2:0]	Input	Register Select
DOUT[7:0]	Output	Data Output Bus
TX	Output	Serial Output Data
DDIS	Output	Driver Disable
RTS_n	Output	Request to Send
DTR_n	Output	Data Terminal Ready
OUT1_n	Output	Output 1
OUT2_n	Output	Output 2
IRQ	Output	Interrupt pending
BAUD_OUT	Output	Baud Out
RX_READY	Output	Receiver Ready to Receive Transmissions
TX_READY	Output	Transmitter Ready to Transmit Data

Table 2: UART 16550 I/O Signals.

Core Assumptions

The 16550 core is modelled after the Texas Instruments 16550. The following differentiate the 16550 from the Texas Instruments device:

- No provision is made for a crystal. The CLK input is designed to accept a standard digital input.

- The bi-directional Data Bus has been split into an input and an output component. To use the core with a bi-directional Data Bus, the DDIS signal can be used as the controlling signal for the tri-state drivers.

- RD2, WR2, CS1 and CS2 have been eliminated. A single signal takes their place. These are RD, WR and CS.

- The ADSN signal has been removed. The 16550 functions as if the ADSN signal is held low. The included wrapper can be used to add the ADSN functionality latching the address and data buses.

- The main clock input CLK must be active from power up.

- The Baudrate Generator is reset to the 0001h value upon activation of the MR signal. Programming the BRG to 0000h is an illegal value. The minimum value for the BRG is 0001h. Until the BRG is programmed, no output is generated.

- The Output Data Bus always shows the value of the last register read.

Verification Methods

The 16550 UART core's functionality has been extensively tested with a testbench and a large number of test patterns. The UART core has also been tested on hardware in several applications.

Design Services

RealFast also offers core integration, core customisation and other design services.

Ordering Information

This product is available from RealFast Intellectual Property AB, under terms of the SignOnce IP License. See www.realfast.se for pricing or contact RealFast for additional information about this product.

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