# HEF4521B

## 24-stage frequency divider and oscillator

Rev. 04 — 21 April 2009

**Product data sheet**

## 1. General description

The HEF4521B consists of a chain of 24 toggle flip-flops with an overriding asynchronous master reset input (MR), and an input circuit that allows three modes of operation. The single inverting stage (A2 to Y2) will function as: a crystal oscillator, an input buffer for an external oscillator or in combination with A1 as an RC oscillator. The crystal oscillator operates in Low-power mode when pins $V_{SS1}$ and $V_{DD1}$ are supplied via external resistors.

Each flip-flop divides the frequency of the previous flip-flop by two, consequently the HEF4521B will count up to $2^{24} = 16777216$. The counting advances on the HIGH-to-LOW transition of the clock (A2). The outputs from each of the last seven stages ($2^{18}$ to $2^{24}$) are available for additional flexibility.

It operates over a recommended $V_{DD}$ power supply range of 3 V to 15 V referenced to $V_{SS}$ (usually ground). Unused inputs must be connected to $V_{DD}$, $V_{SS}$, or another input. It is also suitable for use over the full industrial (−40 °C to +85 °C) temperature range.

## 2. Features

- Low power crystal oscillator operation
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Operates across the full industrial temperature range −40 °C to +85 °C
- Complies with JEDEC standard JESD 13-B
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
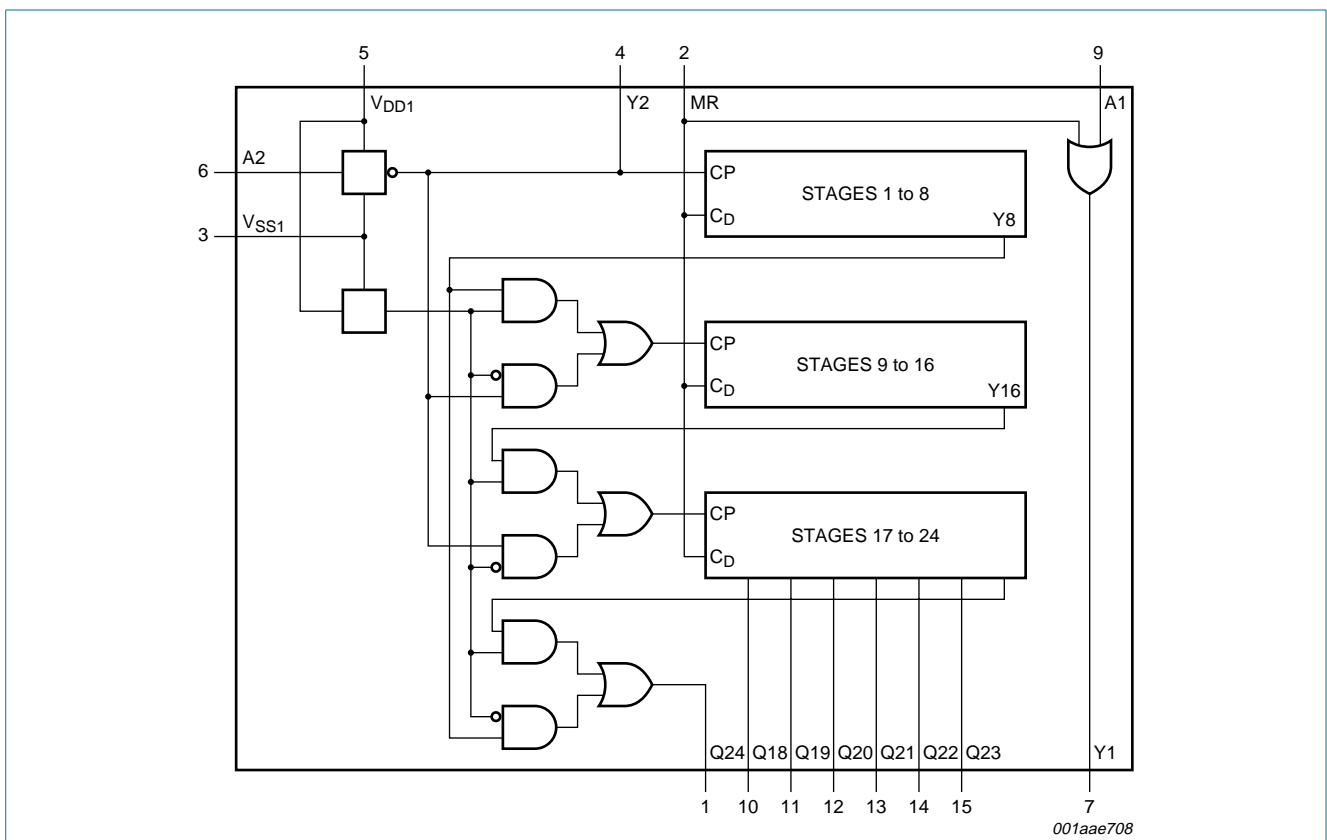  - MM JESD22-A115-A exceeds 200 V

## 3. Applications
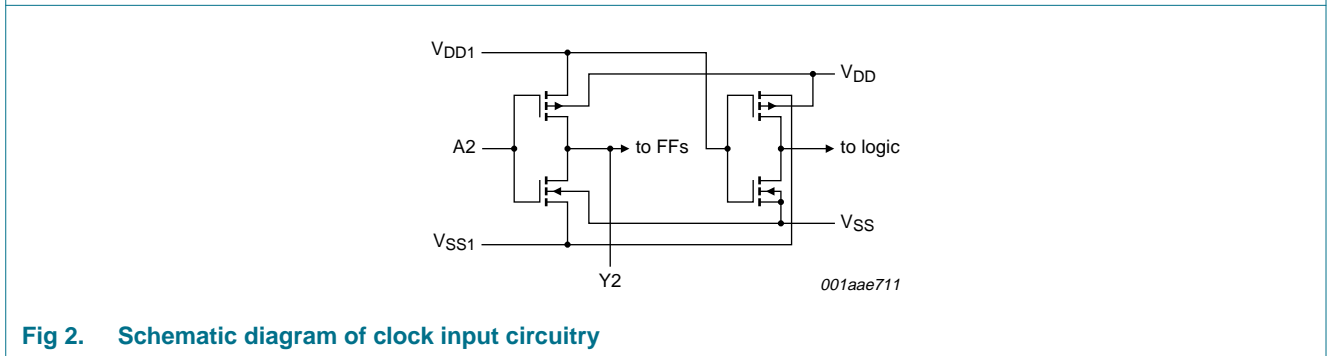
- Industrial

founded by Philips

## 4. Ordering information

**Table 1.    Ordering information**
*All types operate from −40 °C to +85 °C.*

| Type number | Package | | | |
|---|---|---|---|---|
| | **Name** | **Description** | | **Version** |
| HEF4521BP | DIP16 | plastic dual in-line package; 16-leads (300 mil) | | SOT38-4 |
| HEF4521BT | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | | SOT109-1 |

## 5. Functional diagram



**Fig 1.    Functional diagram**



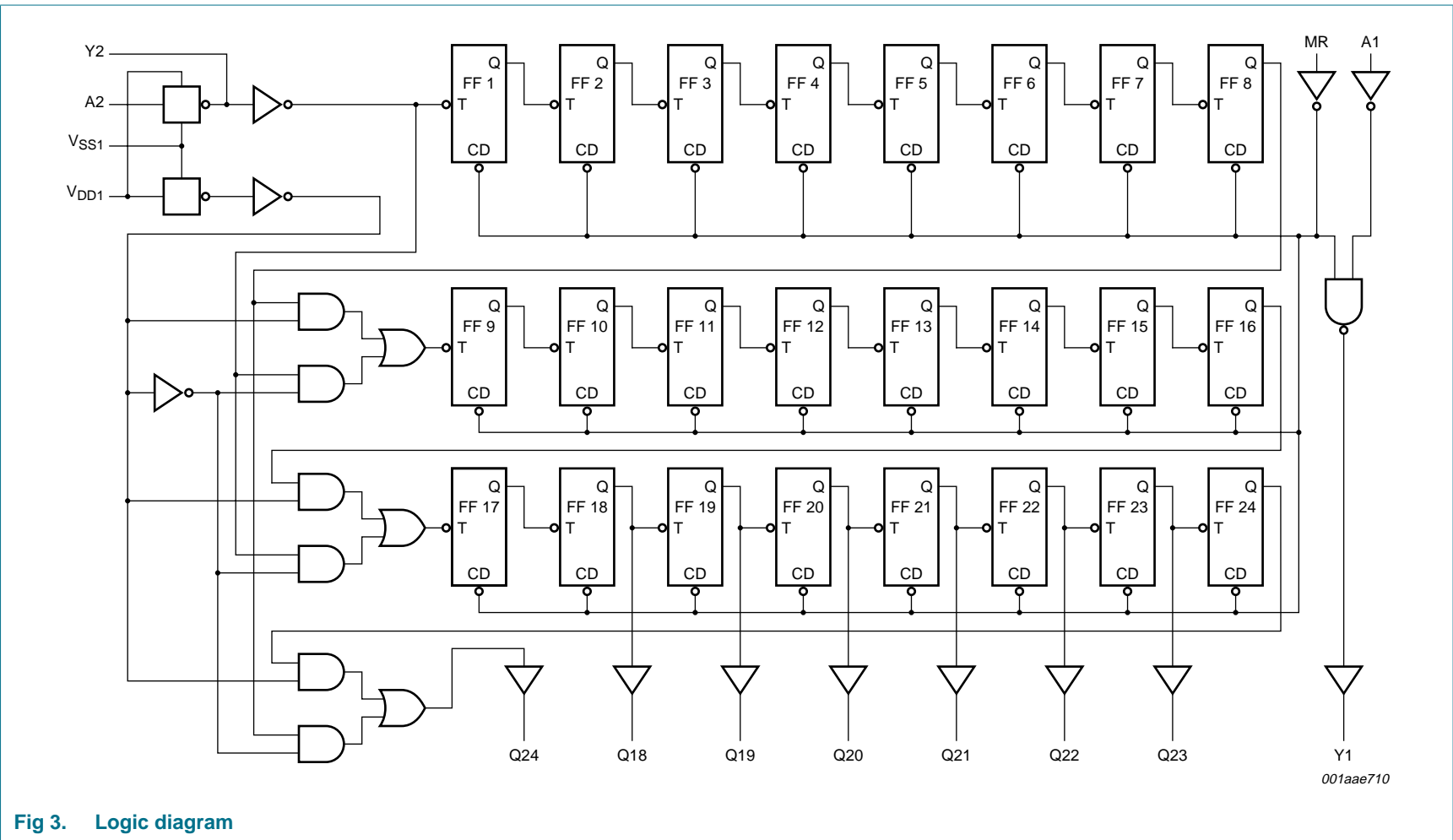**Fig 2.    Schematic diagram of clock input circuitry**

24-stage frequency divider and oscillator

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**Fig 3.** Logic diagram

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## 6. Pinning information

### 6.1 Pinning

**HEF4521B**

| | | | |
|---|---|---|---|
| Y24 | 1 | 16 | V<sub>DD</sub> |

Y24 — 1     16 — V_DD
MR — 2     15 — Q23
V_SS1 — 3     14 — Q22
Q2 — 4     13 — Q21
V_DD1 — 5     12 — Q20
Y2 — 6     11 — Q19
Y1 — 7     10 — Q18
V_SS — 8     9 — A1

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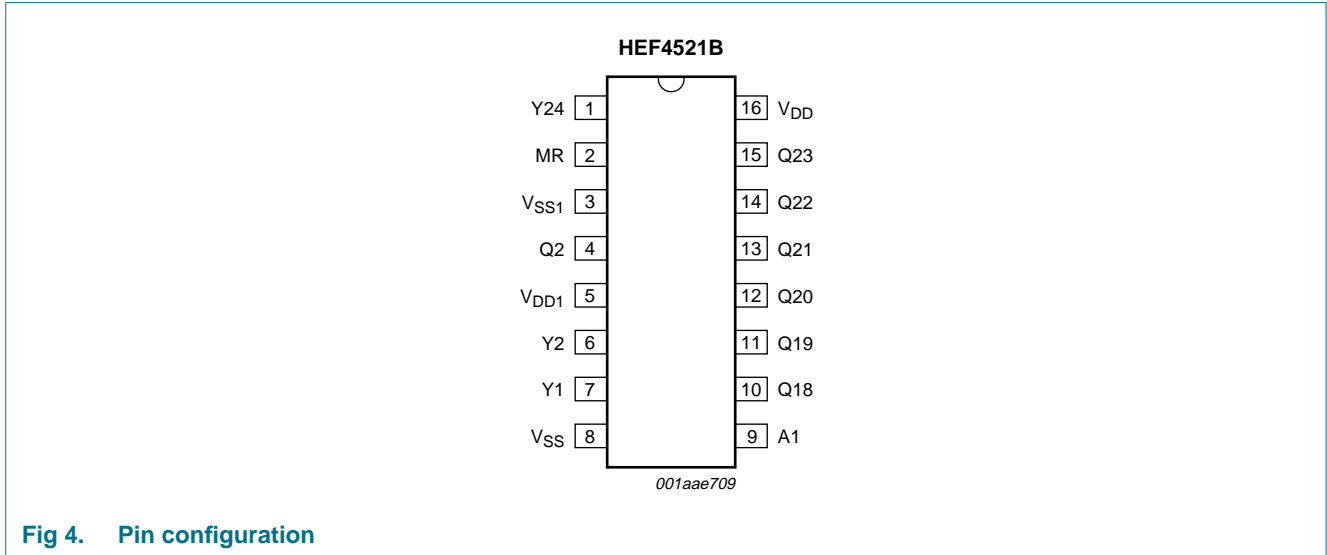
**Fig 4.  Pin configuration**

### 6.2 Pin description

**Table 2.  Pin description**

| Symbol | Pin | Description |
|---|---|---|
| MR | 2 | master reset input |
| $V_{SS1}$ | 3 | ground supply voltage 1 |
| $V_{DD1}$ | 5 | supply voltage 1 |
| Y1, Y2 | 7, 4 | external oscillator connection |
| $V_{SS}$ | 8 | ground supply voltage |
| A1, A2 | 9, 6 | external oscillator connection |
| Q18 to Q24 | 10, 11, 12, 13, 14, 15, 1 | output |
| $V_{DD}$ | 16 | supply voltage |

## 7. Count capacity

**Table 3.  Count capacity**

| Output | Count capacity |
|---|---|
| Q18 | $2^{18} = 262144$ |
| Q19 | $2^{19} = 524288$ |
| Q20 | $2^{20} = 1048576$ |
| Q21 | $2^{21} = 2097152$ |
| Q22 | $2^{22} = 4194304$ |
| Q23 | $2^{23} = 8388608$ |
| Q24 | $2^{24} = 16777216$ |

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## 8. Functional Test

A test function has been included to reduce the test time required to test all 24 counter stages. This test function divides the counter into three 8-stage sections by connecting $V_{SS1}$ to $V_{DD}$ and $V_{DD1}$ to $V_{SS}$. 255 counts are loaded into each of the 8-stage sections in parallel via A2 (connected to Y2). All flip-flops are now at a HIGH level. The counter is now returned to the normal 24-stage in series configuration by connecting $V_{SS1}$ to $V_{SS}$ and $V_{DD1}$ to $V_{DD}$. Entering one more pulse into input A2 will cause the counter to ripple from an all HIGH state to an all LOW state.

**Table 4.  Functional test sequence**

| Inputs | | Control terminals | | | Outputs | Remarks |
|---|---|---|---|---|---|---|
| MR | A2 | Y2 | $V_{SS1}$ | $V_{DD1}$ | Q18 to Q24 | |
| H | L | L | $V_{DD}$ | $V_{SS}$ | L | counter is in three 8-stage sections in parallel mode; A2 and Y2 are interconnected (Y2 is now input); counter is reset by MR. |
| L | see Remarks column | see Remarks column | $V_{DD}$ | $V_{SS}$ | H | 255 pulses are clocked into A2, Y2. The counter advances on the LOW to HIGH transition. |
| L | L | L | $V_{SS}$ | $V_{SS}$ | H | $V_{SS1}$ is connected to $V_{SS}$. |
| L | H | L | $V_{SS}$ | $V_{SS}$ | H | the input A2 is made HIGH. |
| L | H | L | $V_{SS}$ | $V_{DD}$ | H | $V_{DD1}$ is connected to $V_{DD}$; Y2 is now made floating and becomes an output; the device is now in the $2^{24}$ mode. |
| L | ↓ | | $V_{SS}$ | $V_{DD}$ | L | counter ripples from an all HIGH state to an all LOW state. |

[1]    H = HIGH voltage level; L = LOW voltage level; ↓ = HIGH to LOW transition.

## 9. Limiting values

**Table 5.  Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | | | −0.5 | +18 | V |
| $I_{IK}$ | input clamping current | $V_I < -0.5$ V or $V_I > V_{DD} + 0.5$ V | | - | 10 | mA |
| $V_I$ | input voltage | | | −0.5 | $V_{DD} + 0.5$ | V |
| $I_{OK}$ | output clamping current | $V_O < -0.5$ V or $V_O > V_{DD} + 0.5$ V | | - | 10 | mA |
| $I_{I/O}$ | input/output current | | | - | 10 | mA |
| $I_{DD}$ | supply current | to any supply terminal | | - | 100 | mA |
| $T_{stg}$ | storage temperature | | | −65 | +150 | °C |
| $T_{amb}$ | ambient temperature | | | −40 | +85 | °C |
| $P_{tot}$ | total power dissipation | DIP16 package | [1] | - | 750 | mW |
| | | SO16 package | [2] | - | 500 | mW |
| P | power dissipation | per output | | - | 100 | mW |

[1]    For DIP16 package: $P_{tot}$ derates linearly with 12 mW/K above 70 °C.

[2]    For SO16 package: $P_{tot}$ derates linearly with 8 mW/K above 70 °C.

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## 10. Recommended operating conditions

**Table 6.    Recommended operating conditions**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | | 3 | - | 15 | V |
| $V_I$ | input voltage | | 0 | - | $V_{DD}$ | V |
| $T_{amb}$ | ambient temperature | in free air | −40 | - | +85 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{DD}$ = 5 V | - | - | 3.75 | ns/V |
| | | $V_{DD}$ = 10 V | - | - | 0.5 | ns/V |
| | | $V_{DD}$ = 15 V | - | - | 0.08 | ns/V |

## 11. Static characteristics

**Table 7.    Static characteristics**
$V_{SS}$ = 0 V; $V_I$ = $V_{SS}$ or $V_{DD}$ unless otherwise specified.

| Symbol | Parameter | Conditions | $V_{DD}$ | $T_{amb}$ = −40 °C | | $T_{amb}$ = 25 °C | | $T_{amb}$ = 85 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | |
| $V_{IH}$ | HIGH-level input voltage | $\lvert I_O \rvert$ < 1 μA | 5 V | 3.5 | - | 3.5 | - | 3.5 | - | V |
| | | | 10 V | 7.0 | - | 7.0 | - | 7.0 | - | V |
| | | | 15 V | 11.0 | - | 11.0 | - | 11.0 | - | V |
| $V_{IL}$ | LOW-level input voltage | $\lvert I_O \rvert$ < 1 μA | 5 V | - | 1.5 | - | 1.5 | - | 1.5 | V |
| | | | 10 V | - | 3.0 | - | 3.0 | - | 3.0 | V |
| | | | 15 V | - | 4.0 | - | 4.0 | - | 4.0 | V |
| $V_{OH}$ | HIGH-level output voltage | $\lvert I_O \rvert$ < 1 μA | 5 V | 4.95 | - | 4.95 | - | 4.95 | - | V |
| | | | 10 V | 9.95 | - | 9.95 | - | 9.95 | - | V |
| | | | 15 V | 14.95 | - | 14.95 | - | 14.95 | - | V |
| $V_{OL}$ | LOW-level output voltage | $\lvert I_O \rvert$ < 1 μA | 5 V | - | 0.05 | - | 0.05 | - | 0.05 | V |
| | | | 10 V | - | 0.05 | - | 0.05 | - | 0.05 | V |
| | | | 15 V | - | 0.05 | - | 0.05 | - | 0.05 | V |
| $I_{OH}$ | HIGH-level output current | $V_O$ = 2.5 V | 5 V | −1.7 | - | −1.4 | - | −1.1 | - | mA |
| | | $V_O$ = 4.6 V | 5 V | −0.52 | - | −0.44 | - | −0.36 | - | mA |
| | | $V_O$ = 9.5 V | 10 V | −1.3 | - | −1.1 | - | −0.9 | - | mA |
| | | $V_O$ = 13.5 V | 15 V | −3.6 | - | −3.0 | - | −2.4 | - | mA |
| $I_{OL}$ | LOW-level output current | $V_O$ = 0.4 V | 5 V | 0.52 | - | 0.44 | - | 0.36 | - | mA |
| | | $V_O$ = 0.5 V | 10 V | 1.3 | - | 1.1 | - | 0.9 | - | mA |
| | | $V_O$ = 1.5 V | 15 V | 3.6 | - | 3.0 | - | 2.4 | - | mA |
| $I_I$ | input leakage current | | 15 V | - | 0.3 | - | 0.3 | - | 1.0 | μA |
| $I_{DD}$ | supply current | $I_O$ = 0 A | 5 V | - | 20 | - | 20 | - | 150 | μA |
| | | | 10 V | - | 40 | - | 40 | - | 300 | μA |
| | | | 15 V | - | 80 | - | 80 | - | 600 | μA |
| $C_I$ | input capacitance | | - | - | - | - | 7.5 | - | - | pF |

## 12. Dynamic characteristics

**Table 8.    Dynamic characteristics**

$V_{SS} = 0$ V; $T_{amb} = 25\,°C$; for test circuits see Figure 6; unless otherwise specified.

| Symbol | Parameter | Conditions | $V_{DD}$ | | Extrapolation formula | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PHL}$ | HIGH to LOW propagation delay | A2 to Q18; see Figure 5 | 5 V | [1] | 923 ns + (0.55 ns/pF) $C_L$ | - | 950 | 1900 | ns |
| | | | 10 V | | 339 ns + (0.23 ns/pF) $C_L$ | - | 350 | 700 | ns |
| | | | 15 V | | 212 ns + (0.16 ns/pF) $C_L$ | - | 220 | 440 | ns |
| | | Qn to Qn + 1; see Figure 5 | 5 V | | 13 ns + (0.55 ns/pF) $C_L$ | - | 40 | 80 | ns |
| | | | 10 V | | 4 ns + (0.23 ns/pF) $C_L$ | - | 15 | 30 | ns |
| | | | 15 V | | 2 ns + (0.16 ns/pF) $C_L$ | - | 10 | 20 | ns |
| | | MR to Qn | 5 V | | 93 ns + (0.55 ns/pF) $C_L$ | - | 120 | 240 | ns |
| | | | 10 V | | 44 ns + (0.23 ns/pF) $C_L$ | - | 55 | 110 | ns |
| | | | 15 V | | 32 ns + (0.16 ns/pF) $C_L$ | - | 40 | 80 | ns |
| | | A1 to Y1; see Figure 5 | 5 V | | 63 ns + (0.55 ns/pF) $C_L$ | - | 90 | 180 | ns |
| | | | 10 V | | 24 ns + (0.23 ns/pF) $C_L$ | - | 35 | 70 | ns |
| | | | 15 V | | 17 ns + (0.16 ns/pF) $C_L$ | - | 25 | 50 | ns |
| $t_{PLH}$ | LOW to HIGH propagation delay | A2 to Q18; see Figure 5 | 5 V | [1] | 923 ns + (0.55 ns/pF) $C_L$ | - | 950 | 1900 | ns |
| | | | 10 V | | 339 ns + (0.23 ns/pF) $C_L$ | - | 350 | 700 | ns |
| | | | 15 V | | 212 ns + (0.16 ns/pF) $C_L$ | - | 220 | 440 | ns |
| | | Qn to Qn + 1; see Figure 5 | 5 V | | 13 ns + (0.55 ns/pF) $C_L$ | - | 40 | 80 | ns |
| | | | 10 V | | 4 ns + (0.23 ns/pF) $C_L$ | - | 15 | 30 | ns |
| | | | 15 V | | 2 ns + (0.16 ns/pF) $C_L$ | - | 10 | 20 | ns |
| | | A1 to Y1; see Figure 5 | 5 V | | 33 ns + (0.55 ns/pF) $C_L$ | - | 60 | 120 | ns |
| | | | 10 V | | 19 ns + (0.23 ns/pF) $C_L$ | - | 30 | 60 | ns |
| | | | 15 V | | 12 ns + (0.16 ns/pF) $C_L$ | - | 20 | 40 | ns |
| $t_t$ | transition time | Qn; see Figure 5 | 5 V | [1] | 10 ns + (1.00 ns/pF) $C_L$ | - | 60 | 120 | ns |
| | | | 10 V | | 9 ns + (0.42 ns/pF) $C_L$ | - | 30 | 60 | ns |
| | | | 15 V | | 6 ns + (0.28 ns/pF) $C_L$ | - | 20 | 40 | ns |
| $t_W$ | pulse width | A2 HIGH; minimum width; see Figure 5 | 5 V | | | 80 | 40 | - | ns |
| | | | 10 V | | | 40 | 20 | - | ns |
| | | | 15 V | | | 30 | 15 | - | ns |
| | | MR HIGH; minimum width; see Figure 5 | 5 V | | | 70 | 35 | - | ns |
| | | | 10 V | | | 40 | 20 | - | ns |
| | | | 15 V | | | 30 | 15 | - | ns |
| $t_{rec}$ | recovery time | MR; see Figure 5 | 5 V | | | +20 | −10 | - | ns |
| | | | 10 V | | | +15 | −5 | - | ns |
| | | | 15 V | | | 15 | 0 | - | ns |
| $f_{max}$ | maximum frequency | A1; see Figure 5 | 5 V | | | 6 | 12 | - | MHz |
| | | | 10 V | | | 12 | 25 | - | MHz |
| | | | 15 V | | | 17 | 35 | - | MHz |

[1]  The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown ($C_L$ in pF).

**Table 9.** **Dynamic power dissipation $P_D$**

*$P_D$ can be calculated from the formulas shown. $V_{SS} = 0$ V; $t_r = t_f \leq 20$ ns; $T_{amb} = 25\,°C$.*

| Symbol | Parameter | $V_{DD}$ | Typical formula for $P_D$ ($\mu$W) | where: |
|--------|-----------|----------|-----------------------------------|--------|
| $P_D$ | dynamic power dissipation | 5 V | $P_D = 1200 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ | $f_i$ = input frequency in MHz, |
| | | 10 V | $P_D = 5100 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ | $f_o$ = output frequency in MHz, |
| | | 15 V | $P_D = 13050 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ | $C_L$ = output load capacitance in pF, |
| | | | | $V_{DD}$ = supply voltage in V, |
| | | | | $\Sigma(C_L \times f_o)$ = sum of the outputs. |

# 13. Waveforms
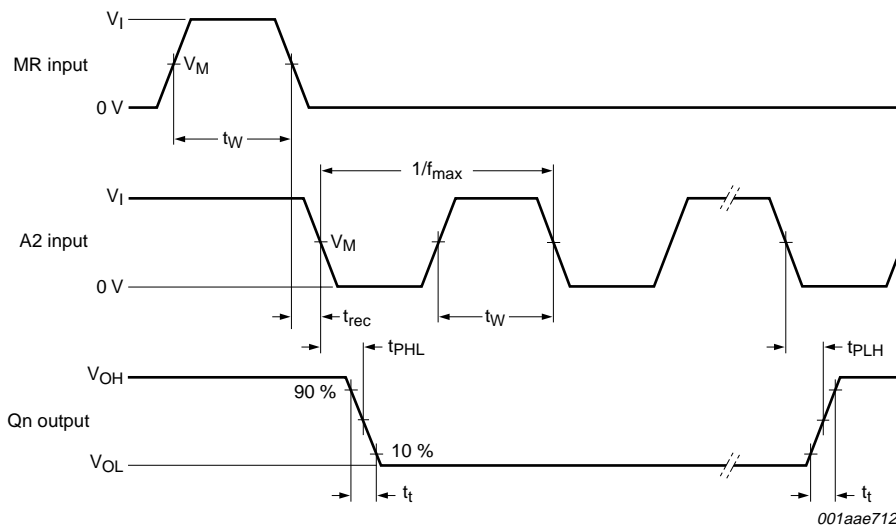


a. Pulse widths, maximum frequency, recovery and transition times and A2 to Qn propagation delays
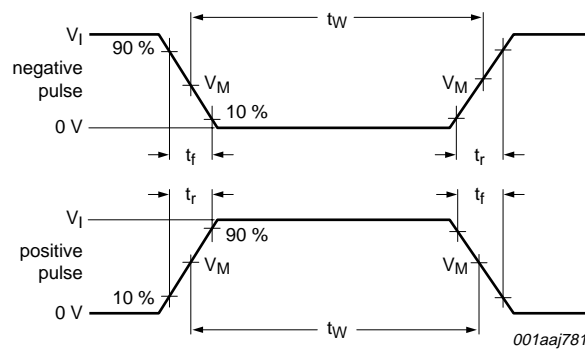


A1 to Y1 or MR to Qn propagation delays

Qn to Qn + 1 propagation delays

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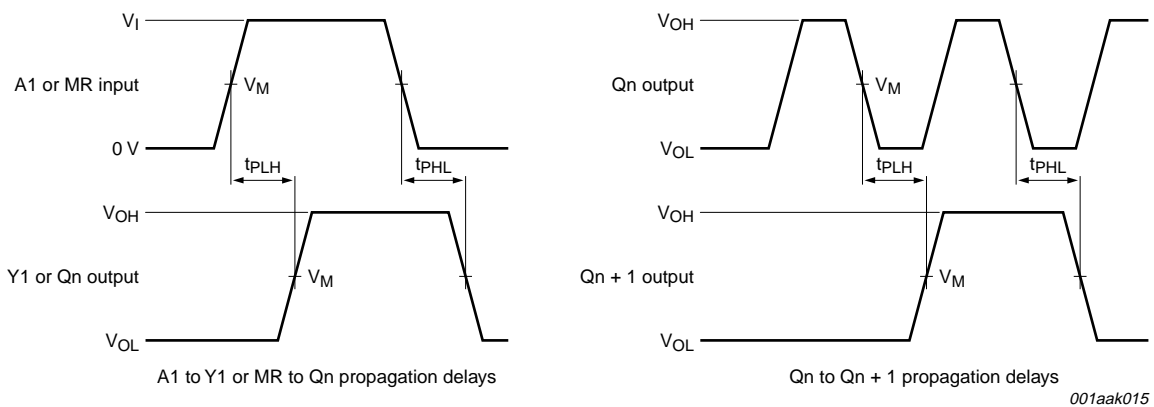
b. A1 to Y1, MR to Qn and Qn to Qn + 1 propagation delays
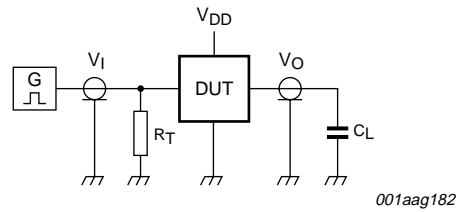
Measurement points are given in Table 10.

The logic levels $V_{OH}$ and $V_{OL}$ are typical output voltage levels that occur with the output load.

**Fig 5.** **Waveforms showing measurement of dynamic characteristics**

a.  Input waveforms



b.  Test circuit

Test data is given in Table 10.

Definitions for test circuit:

$C_L$ = Load capacitance including jig and probe capacitance;

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator.

**Fig 6.    Test circuit for switching times**

**Table 10.    Measurement points and test data**

| Supply voltage | Input | | | Load |
|---|---|---|---|---|
| | $V_I$ | $V_M$ | $t_r$, $t_f$ | $C_L$ |
| 5 V to 15 V | $V_{DD}$ | $0.5V_I$ | ≤ 20 ns | 50 pF |

## 14. Application information



(1) Optional for low power operation.

**Fig 7.    Crystal oscillator circuit**
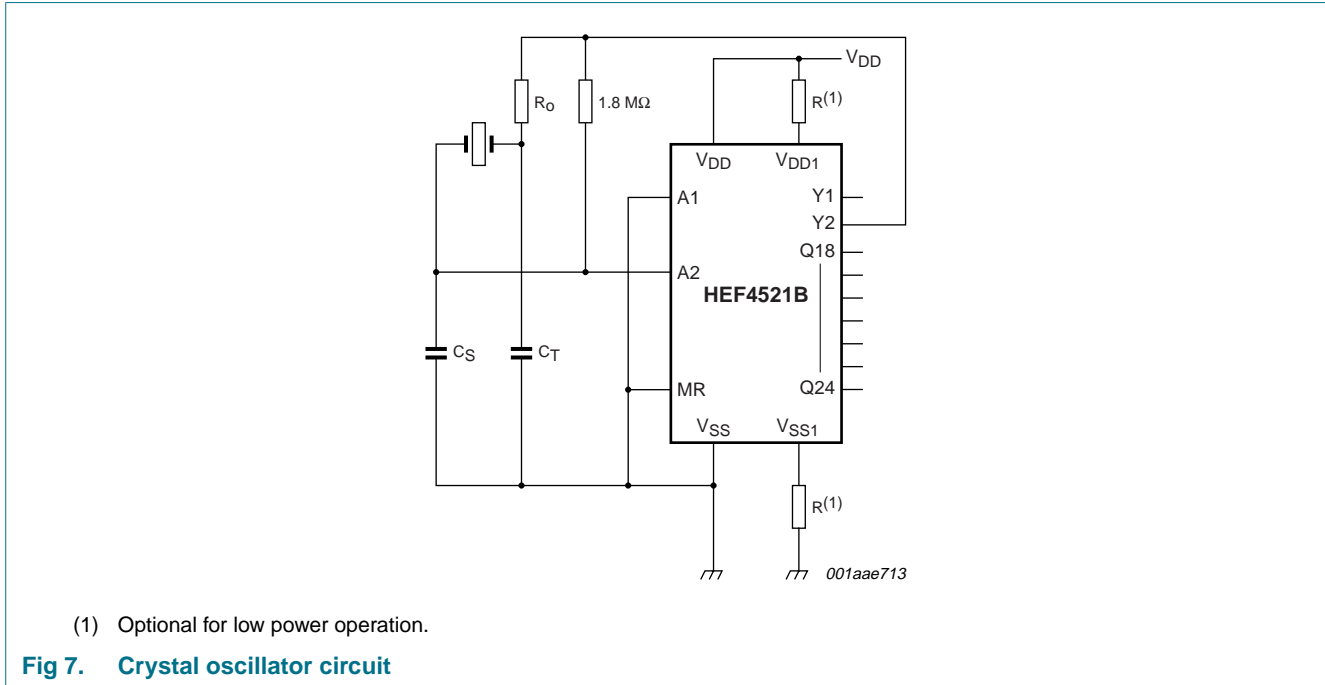
**Table 11.    Typical characteristics for crystal oscillator**
See *Figure 7*.

| Parameter | 500 kHz circuit | 50 kHz circuit | Unit |
|---|---|---|---|
| **Crystal characteristics** | | | |
| Resonance frequency | 500 | 50 | kHz |
| Crystal cut | S | N | - |
| Equivalent resistance; $R_S$ | 1 | 6.2 | kΩ |
| **External resistor/capacitor values** | | | |
| $R_o$ | 47 | 750 | kΩ |
| $C_T$ | 82 | 82 | pF |
| $C_S$ | 20 | 20 | pF |
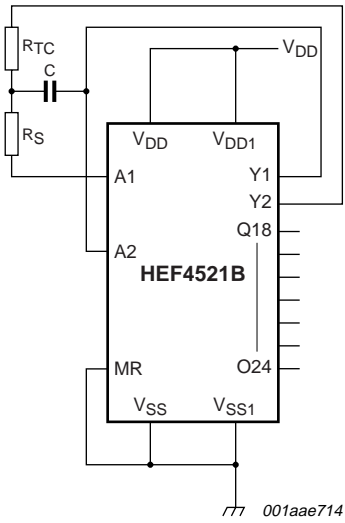
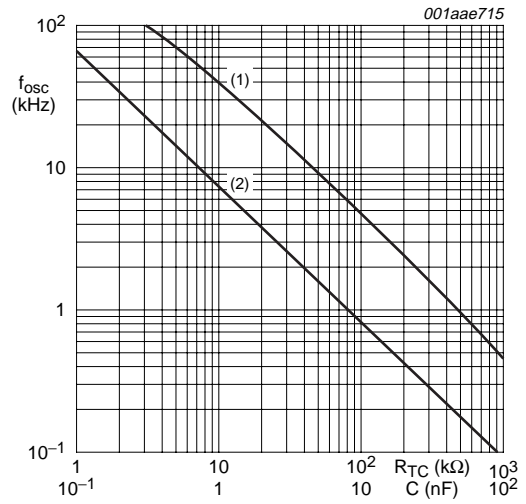$$f \approx \frac{1}{2.3 \times R_{TC} \times C} \; ; \; R_S \geq 2R_{TC} \; , \text{ where:}$$

f is in Hz, R is in $\Omega$, and C is in F.

$$R_S + R_{TC} < \frac{V_{IL(max)}}{I_{LI}} \; , \text{ where:}$$

$V_{IL(max)}$ = maximum input voltage LOW; and
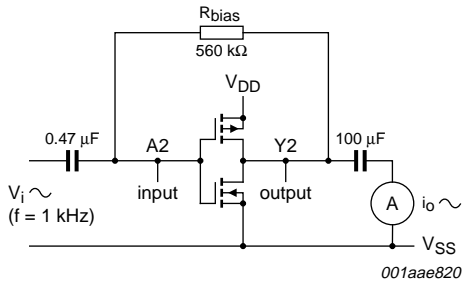
$I_{LI}$ = input leakage current.

**Fig 8.   RC oscillator circuit**
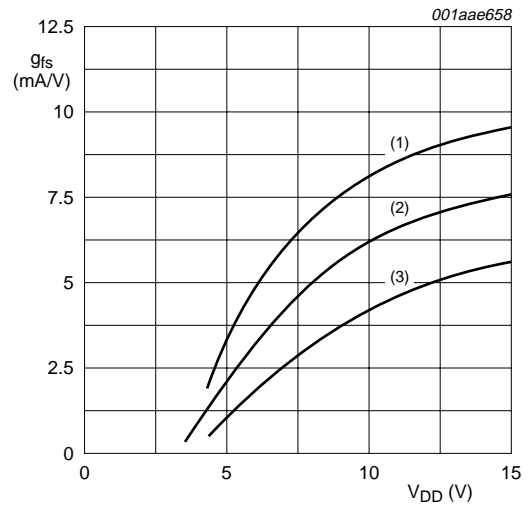


$V_{DD}$ = 10 V; The test circuit is shown in Figure 8.

(1)  $R_{TC}$; C = 1 nF; $R_S \approx 2 R_{TC}$.

(2)  C; $R_{TC}$ = 56 k$\Omega$; $R_S$ = 120 k$\Omega$.

**Fig 9.   Oscillator frequency as a function of $R_{TC}$ and C**

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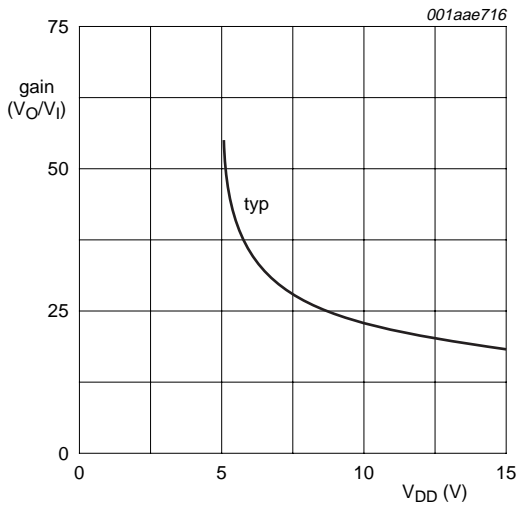**Product data sheet**                **Rev. 04 — 21 April 2009**                                    **11 of 17**

$g_{fs} = d_{io}/d_{vi}$ with $v_o$ constant (see Figure 11).

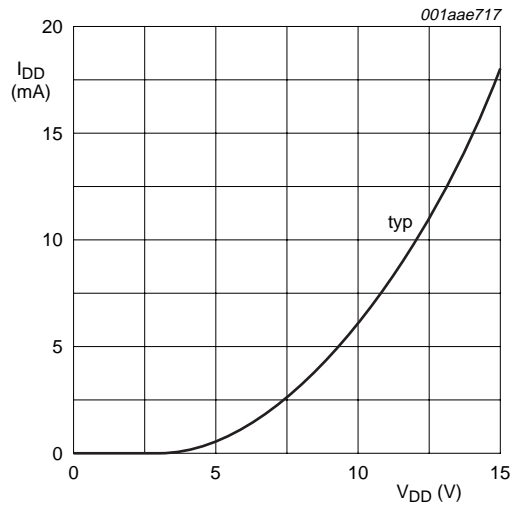**Fig 10. Test setup for measuring forward transconductance**



(1) Average + 2 s.

(2) Average.

(3) Average − 2 s, where 's' is the observed standard deviation.

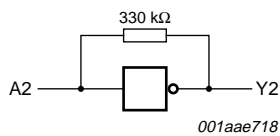**Fig 11. Typical forward transconductance $g_{fs}$ as a function of the supply voltage at $T_{amb} = 25 \ °C$**



**Fig 12. Voltage gain $V_O/V_I$ as a function of supply voltage**



**Fig 13. Supply current as a function of supply voltage**



**Fig 14. Test setup for measuring the Figure 12 and Figure 13 graphs**

## 15. Package outline

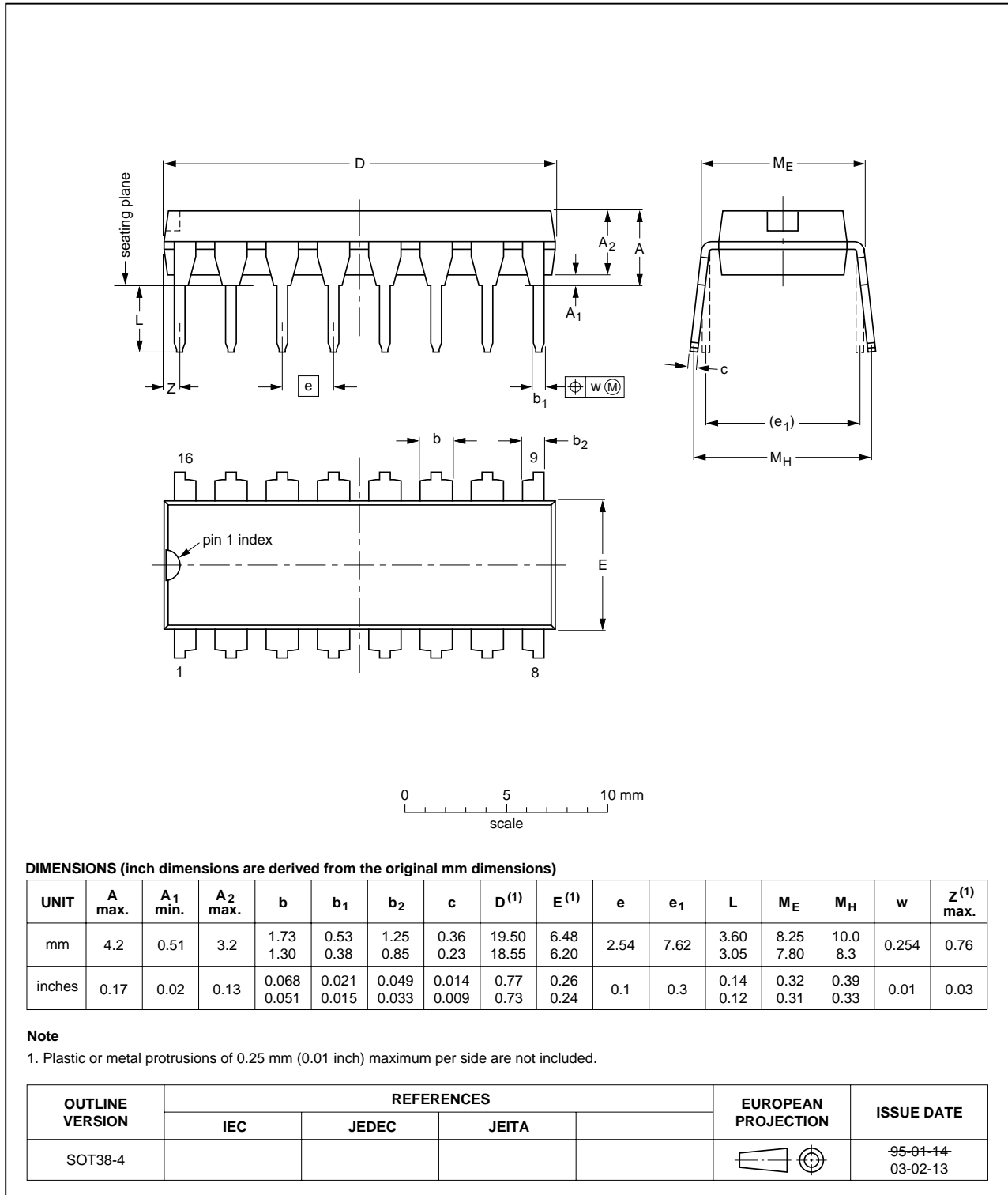**DIP16: plastic dual in-line package; 16 leads (300 mil)**                                              **SOT38-4**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | A₁ min. | A₂ max. | b | b₁ | b₂ | c | D[1] | E[1] | e | e₁ | L | M_E | M_H | w | Z[1] max. |
|------|--------|---------|---------|---|----|----|---|------|------|---|----|---|-----|-----|---|-----------|
| mm | 4.2 | 0.51 | 3.2 | 1.73 1.30 | 0.53 0.38 | 1.25 0.85 | 0.36 0.23 | 19.50 18.55 | 6.48 6.20 | 2.54 | 7.62 | 3.60 3.05 | 8.25 7.80 | 10.0 8.3 | 0.254 | 0.76 |
| inches | 0.17 | 0.02 | 0.13 | 0.068 0.051 | 0.021 0.015 | 0.049 0.033 | 0.014 0.009 | 0.77 0.73 | 0.26 0.24 | 0.1 | 0.3 | 0.14 0.12 | 0.32 0.31 | 0.39 0.33 | 0.01 | 0.03 |

**Note**

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|--|--|--|---------------------|------------|
| | IEC | JEDEC | JEITA | | | |
| SOT38-4 | | | | | | 95-01-14 03-02-13 |

**Fig 15. Package outline SOT38-4 (DIP16)**

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**SO16: plastic small outline package; 16 leads; body width 3.9 mm** **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT | A max. | A₁ | A₂ | A₃ | b_p | c | D[1] | E[1] | e | H_E | L | L_p | Q | v | w | y | Z[1] | θ |
|------|--------|----|----|----|-----|---|------|------|---|-----|---|-----|---|---|---|---|------|---|
| mm | 1.75 | 0.25 0.10 | 1.45 1.25 | 0.25 | 0.49 0.36 | 0.25 0.19 | 10.0 9.8 | 4.0 3.8 | 1.27 | 6.2 5.8 | 1.05 | 1.0 0.4 | 0.7 0.6 | 0.25 | 0.25 | 0.1 | 0.7 0.3 | 8° 0° |
| inches | 0.069 | 0.010 0.004 | 0.057 0.049 | 0.01 | 0.019 0.014 | 0.0100 0.0075 | 0.39 0.38 | 0.16 0.15 | 0.05 | 0.244 0.228 | 0.041 | 0.039 0.016 | 0.028 0.020 | 0.01 | 0.01 | 0.004 | 0.028 0.012 | |

**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|--------|-------|--|---------------------|------------|
| | IEC | JEDEC | JEITA | | | |
| SOT109-1 | 076E07 | MS-012 | | | | ~~99-12-27~~ 03-02-19 |

**Fig 16.  Package outline SOT109-1 (SO16)**

## 16. Abbreviations

**Table 12.    Abbreviations**

| Acronym | Description |
|---------|-------------|
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |

## 17. Revision history

**Table 13.    Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-------------|--------------|-------------------|---------------|------------|
| HEF4521B_4 | 20090421 | Product data sheet | - | HEF4521B_CNV_3 |
| Modifications: | <ul><li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>Legal texts have been adapted to the new company name where appropriate.</li><li>Section 2 "Features" added.</li><li>Section 3 "Applications" added.</li><li>Package version SOT38-1 changed to SOT38-4 in Section 4, and Figure 15. Package SOT74 removed from Section 4.</li><li>Section 9 "Limiting values" and Section 11 "Static characteristics" added, taken from the HE4000B Family Specifications data sheet.</li><li>Section 16 "Abbreviations" added.</li></ul> | | | |
| HEF4521B_CNV_3 | 19950101 | Product specification | - | HEF4521B_CNV_2 |
| HEF4521B_CNV_2 | 19950101 | Product specification | - | - |

# 18. Legal information

## 18.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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# 20. Contents