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Application Note AD-04

Reducing the Power Requirements of Comlinear CLC949 Support Circuitry

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Introduction

If you have to design a system requiring low power dissipation and high performance data acquisition you would naturally be attracted to the Comlinear CLC949 A/D converter. The CLC949 is a low power, 12 bit A/D Converter capable of achieving 30MSPS sample rates and accurately digitizing signals at high frequencies. At a sample rate of 20MSPS, the CLC949 dissipates very little power: 220mW. Anxious to try out this new converter, you order an evaluation board and begin to put it through its paces. You soon realize that although the A/D converter dissipates very little power, the support circuitry on the board exceeds your power budget. The reason for this is that the evaluation board was designed as a general purpose board which can handle a broad range of input signal types, and clock types, always providing the best possible performance. The purpose of the board is to show off the performance of the A/D converter, not the support circuitry. In most systems, this circuitry is not optimal from a system standpoint, where other factors such as parts count and total power dissipation need to be taken into consideration. For these applications we will explore alternative circuits for the input driver and clock generator which dissipate far less power than those that are provided on the evaluation board, and we will explore the performance trade-offs that these circuits offer.

Driving the input

The CLC949 has a differential input. If your system uses a fully differential signal, then it is possible that no additional circuitry will be required to drive the CLC949. In many systems the signal that needs to be digitized is single ended. The result is that these systems must contain single-ended-to-differential drivers. The lowest power (none), lowest cost and lowest distortion circuit that can provide this is an RF transformer such as the TM01-1T from Mini-Circuits. The one disadvantage that this option has is that it cannot operate with input frequencies below about 50kHz. For applications that require a DC coupled input, the evaluation board was fitted with an op amp- based circuit that provides the lowest possible distortion for high frequency inputs through 15MHz. That circuit uses a CLC428 Dual, Low Noise Op Amp to generate the DC biases required in the circuit, and two high speed CLC409 op amps in the signal path. The CLC409 offers exceptionally low distortion which causes it to burn large amounts of power. To further improve the distortion of the CLC409 in this application, pull-up resistors were added to the outputs of the op amp. A total of 38mW is dissipated in these resistors alone, the CLC409 uses 135mW each, and the CLC428 uses another 110mW, for a total of about 420mW being dissipated in the input driver circuit.

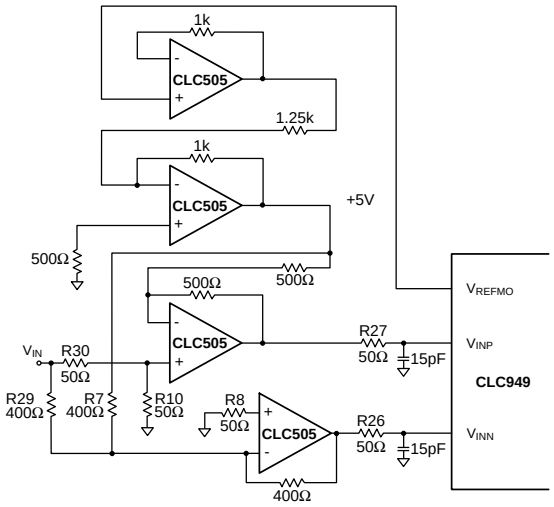

Figure 1

An alternative for systems which do not have input signals that extend up to 15MHz, or in which distortion at these frequencies is not as important, is the use of a circuit based on the CLC505 High Speed, Programmable Supply Current Op Amp. The same circuit that is used on the evaluation board but with four CLC505's substituted for the four op amps in the circuit can be used. By powering each CLC505 at a level of 1mA, the total power drain of this circuit is about 40mW or 10% of what the standard circuit on the evaluation board uses. But the big question is "How much do I give up in performance when I take advantage of this low power input driver?" The answer is "not much" in most cases.

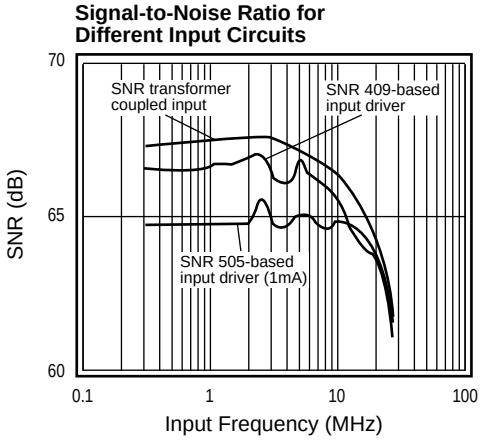

Figure 2a

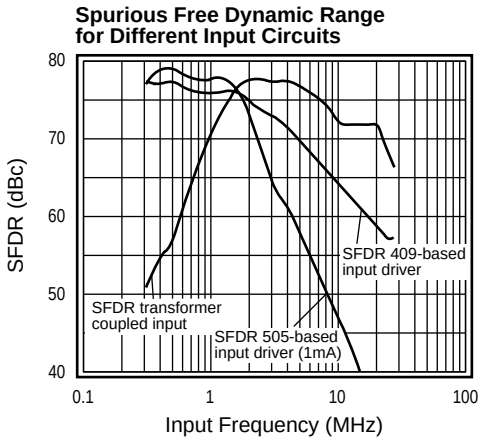

Figure 2b

In Figure 2a and 2b, it can be seen that for low input frequencies (below 1.5MHz) the amplifier-based input circuits offer the lowest distortion, but as the input frequencies rise above 1.5MHz, the distortion degrades. The distortion degrades faster for the CLC505-based circuit than the CLC409-based circuit that is on the evaluation board. At higher input frequencies, the transformer coupled input is clearly the superior choice.

In many applications, far more important than distortion, is the noise performance of the converter. The lowest noise circuit, with SNR of 67dB, is the transformer coupled input. The next lowest noise is the circuit that is used on the evaluation board which uses the CLC428 dual, low noise amplifier to generate the offset reference voltages. Using the CLC428 rather than the transformer costs you about one dB in noise performance. By substituting the CLC505 for the CLC428, we reduce the power in this part of the circuit (from about 110mW to about 20mW) but we must pay the price with higher noise - an SNR of about 64dB.

With the CLC505, there are other trade-offs that can be made in that you have control over the bias currents within the CLC505 op amp. As the bias current is turned up, the bandwidth of the op amp increases, and its distortion decreases. For more information on the CLC505, please refer to the CLC505 data sheet. In Figure 3a and 3b, you can see the impact of increasing the bias current of the CLC505 is to lower the rate of distortion degradation as the input frequency increases.

Clock Generation

When sampling a high speed input signal, a dominant source of noise is the noise generated by the aperture jitter. This jitter is contributed partially by the converter itself and partially by the clock generation circuitry. The circuit that is used on the CLC949 evaluation board was designed to allow a broad range of clock signals, from high slew rate square waves to low slew rate sinusoids, and uses a CLC006 cable driver which operates as a very low jitter comparator. When sampling input signals with a low slew rate, the jitter is not a major source of noise, and this provides us with another opportunity for power reduction. In all of the data, where the CLC505 has been used as the input buffer, the CLC006 had been removed from the board and there was a jumper between pin 1 and pin 7 of the CLC006 socket. This makes the 74HC04 act as the clock generator, with the sinusoidal clock input biased mid-way between the supplies. When a low jitter, high slew rate, CMOS level clock is available, no external clock conditioning circuitry is required, and therefore no extra power is dissipated.

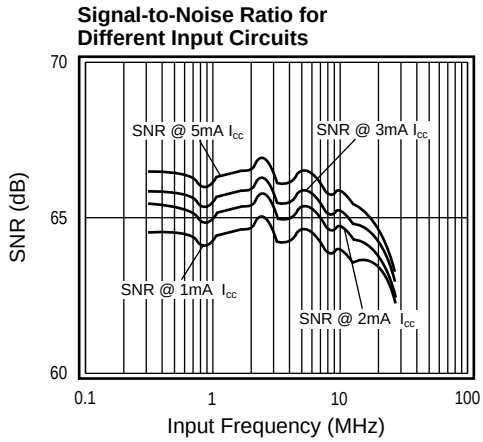

Figure 3a

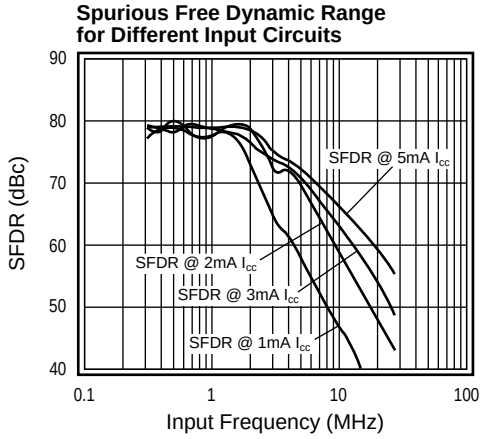

Figure 3b

Conclusion

The primary design goal when developing the CLC949 evaluation board was to gain the maximum versatility and to provide good performance with a broad range of input signals and clock sources. In a final application circuit design, there are significant opportunities for reducing the power dissipation in the support circuitry surrounding the CLC949. The key to optimizing the performance of the CLC949 in your application is to clearly understand the requirements, and select support circuitry that meets these requirements efficiently.

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