NEC

MOS INTEGRATED CIRCUIT
μPD17P133

SMALL GENERAL-PURPOSE 4 BIT SINGLE-CHIP MICROCONTROLLER

The μPD17P133 is a one-time PROM version of the μPD17133, in which the internal masked ROM of the μPD17133 is replaced with a one-time PROM that can be written to just once.

Since user programs can be written to the PROM, this microcontroller is suited for program evaluation and small-lot production of the μPD17121/μPD17133, or for program evaluation of the μPD17133(A).

The following user's manual completely describes the functions of the μPD17P133. Be sure to read it before designing an application system.

μPD17120 Sub-Series User's Manual: IEU-1367

FEATURES

- 17K architecture : General registers
- Upward compatible with the μPD17121
- Pin compatible with the μPD17133 (except for PROM programming function)
- Internal one-time PROM: 2K bytes (1024 × 16 bits)
- Supply voltage : V_{DD} = 2.7 to 5.5 V (f_X = 400 kHz to 4 MHz)
  V_{DD} = 4.5 to 5.5 V (f_X = 400 kHz to 8 MHz)

ORDERING INFORMATION

Part number	Package
μPD17P133CS	24-pin plastic shrink DIP (300 mil)
μPD17P133GT	24-pin plastic SOP (375 mil)

The information in this document is subject to change without notice.

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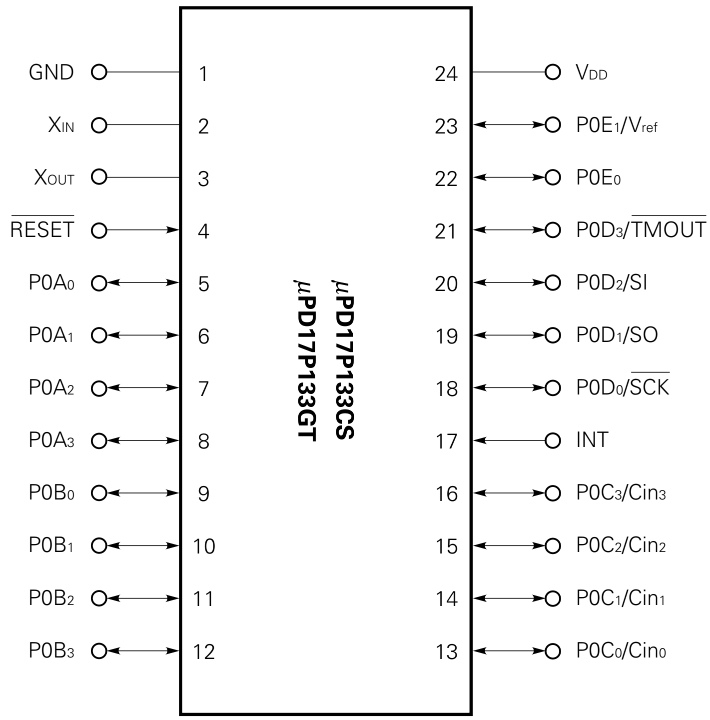
Major changes in this revision are indicated by stars (★) in the margins.

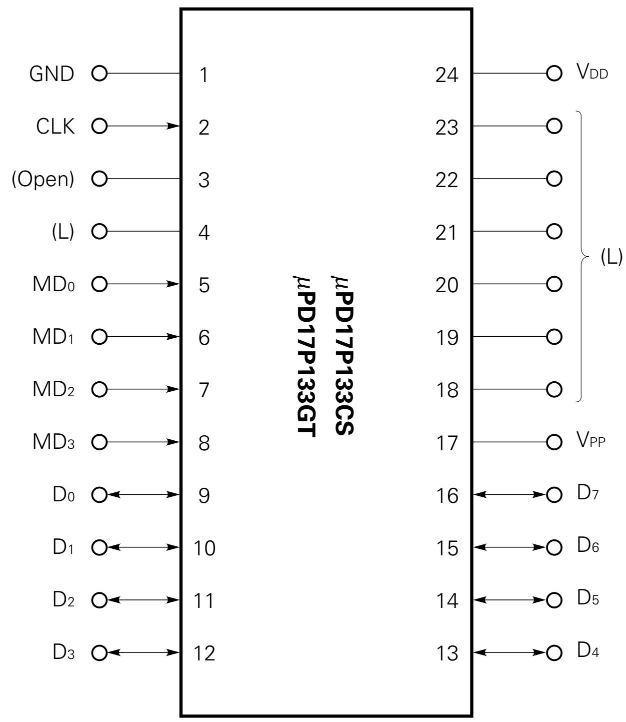
PIN CONFIGURATION (TOP VIEW)

(1) Normal operating mode



Cin_0-Cin_3	:	Comparator input
GND	:	Ground
INT	:	External interrupt input
$P0A_0$-$P0A_3$	:	Port 0A
$P0B_0$-$P0B_3$	:	Port 0B
$P0C_0$-$P0C_3$	:	Port 0C
$P0D_0$-$P0D_3$	:	Port 0D
$P0E_0$, $P0E_1$	:	Port 0E
RESET	:	Reset input
SCK	:	Serial clock input/output
SI	:	Serial data input
SO	:	Serial data output
TMOUT	:	Timer output
V_{DD}	:	Positive power supply
V_{ref}	:	External reference voltage input
X_{IN}, X_{OUT}	:	System clock oscillation

(2) Program memory write/verify mode



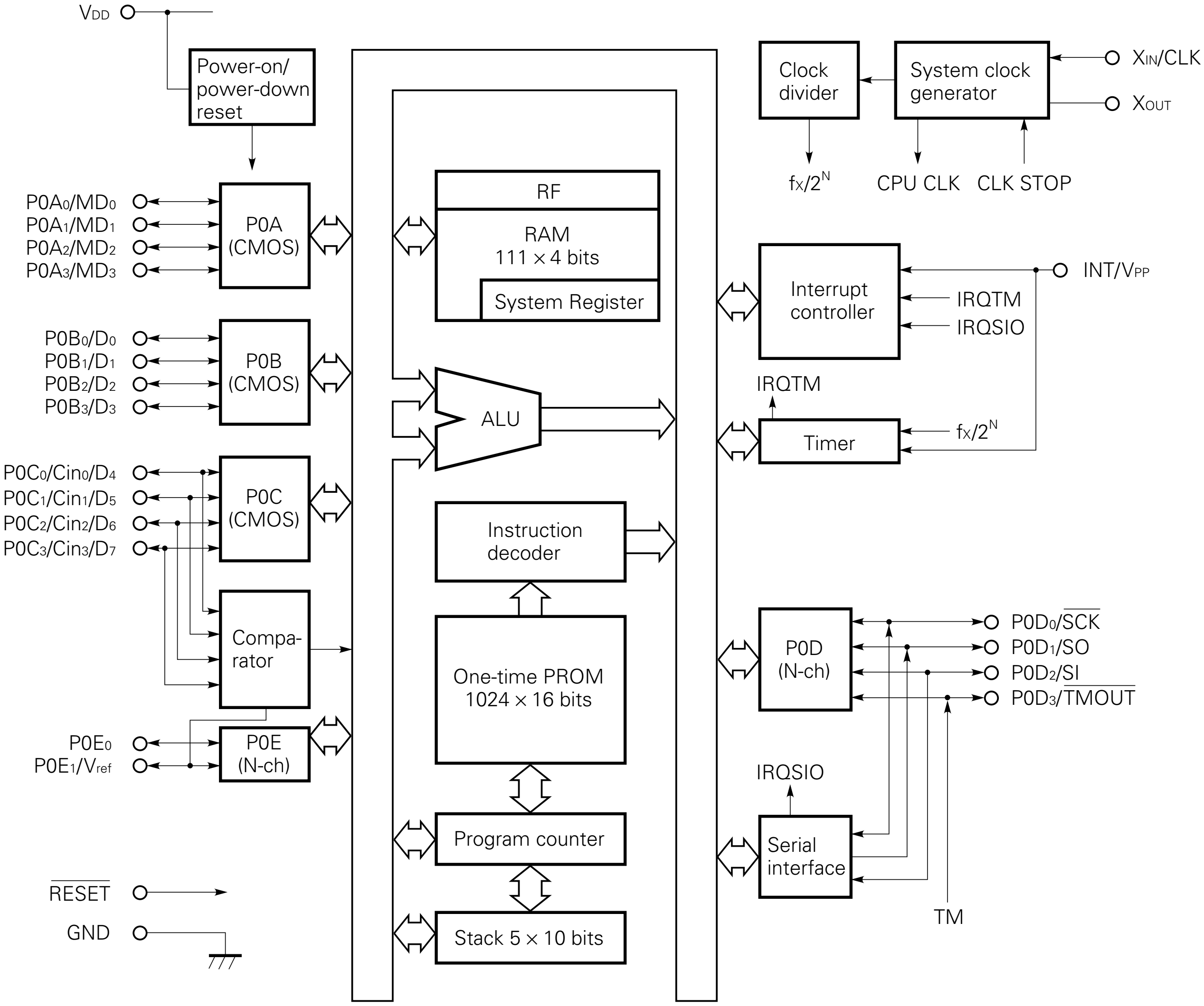
CLK	: Address update clock input	MD_0-MD_3	: Operation mode selection input
D_0-D_7	: Data input/output	V_{DD}	: Power supply
GND	: Ground	V_{PP}	: Programming power supply

Caution Symbols in parentheses denote processing for pins not used in the program memory write/verify mode.

L: Connect these pins separately to the GND pin through pull-down resistors.

Open: Nothing should be connected on these pins.

BLOCK DIAGRAM



Remark The terms CMOS and N-ch in parentheses indicate the output form of the port.

CMOS: CMOS push-pull output

N-ch: N-channel open-drain output

CONTENTS

1. PIN FUNCTIONS

1.1 NORMAL OPERATION MODE

Pin No.	Pin name	Function	Output	At reset
1	GND	Ground	–	–
2 3	X_{IN} X_{OUT}	For system clock oscillation. Ceramic resonator is connected with these pins.	–	–
4	$\overline{RESET}$	System reset input pin	–	Input
5 to 8	$P0A_0$ to $P0A_3$	Port 0A · 4-bit input/output port · Input/output setting allowed in units of 1 bit	CMOS push-pull	Input
9 to 12	$P0B_0$ to $P0B_3$	Port 0B · 4-bit input/output port · Input/output setting allowed in units of 4 bits	CMOS push-pull	Input
13 to 16	$P0C_0/Cin_0$ to $P0C_3/Cin_3$	Port 0C. Analog voltage is supplied to the comparator through these pins. • $P0C_0$ - $P0C_3$ · 4-bit input/output port · Input/output setting allowed in units of 1 bit • Cin_0 - Cin_3 · Analog input for the comparator	CMOS push-pull	Input (P0C)
17	INT	External interrupt request or sensor signal	–	Input
18 19 20 21	$P0D_0/\overline{SCK}$ $P0D_1/SO$ $P0D_2/SI$ $P0D_3/\overline{TMOUT}$	Pin for port 0D, timer carry output, serial data input, serial data output, and serial clock input/output • $P0D_0$ - $P0D_3$ · 4-bit input/output port · Input/output setting allowed in units of 1 bit • $\overline{SCK}$ · Serial clock input/output • SO · Serial data output • SI · Serial data input • $\overline{TMOUT}$ · Timer output	N-ch open drain	Input (P0D)
22 23	$P0E_0$ $P0E_1/V_{ref}$	Port 0E. Reference voltage is supplied to the comparator through these pins. Withstand voltage of $P0E_1$ is V_{DD} (MAX.). • $P0E_0$ and $P0E_1$ · 2-bit input/output port · Input/output setting allowed in units of 1 bit • V_{ref} · Input of external reference voltage for the comparator	N-ch open drain	Input (P0E)
24	V_{DD}	Power supply pin	–	–

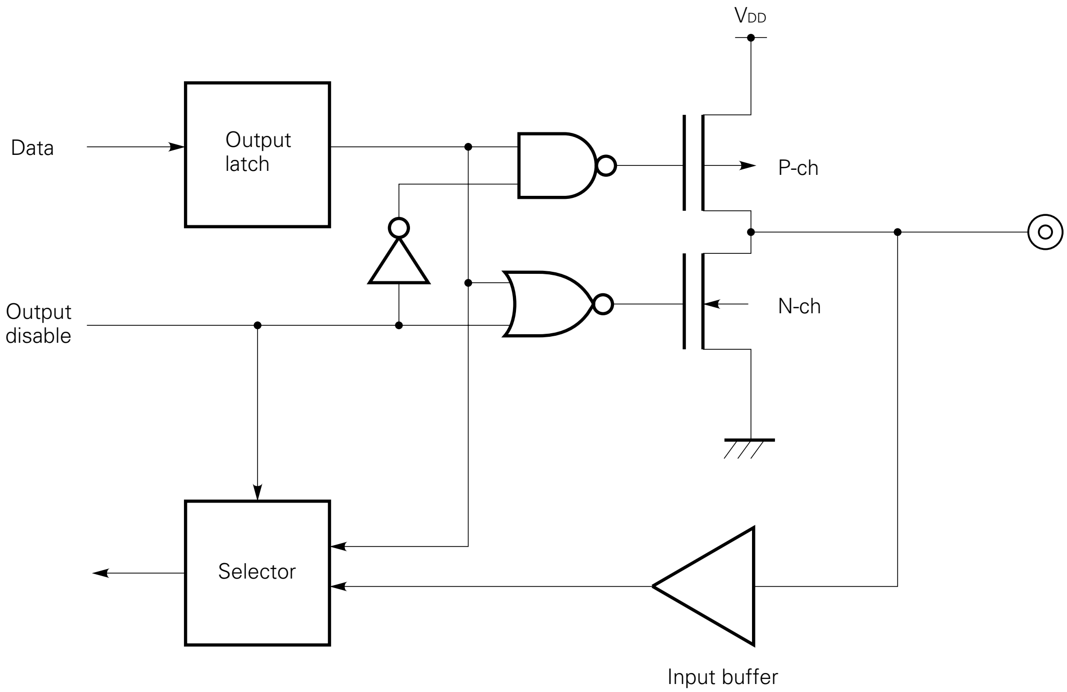
1.2 PROGRAM MEMORY WRITE/VERIFY MODE

Pin No.	Pin name	Function	Input/output
1	GND	Ground	–
2	CLK	Input pin for address update clocks used when writing to program memory or verifying its contents	Input
5 to 8	MD_0 to MD_3	Input pins that select an operation mode when writing to program memory or verifying its contents	Input
9 to 16	D_0 to D_7	Input/output pins for 8-bit data used when writing to program memory or verifying its contents	Input/output
17	V_{PP}	Voltage (+12.5 V) is applied to this pin when writing to program memory or verifying its contents.	–
24	V_{DD}	Power supply pin. +6 V is applied to this pin when writing to program memory or verifying its contents.	–

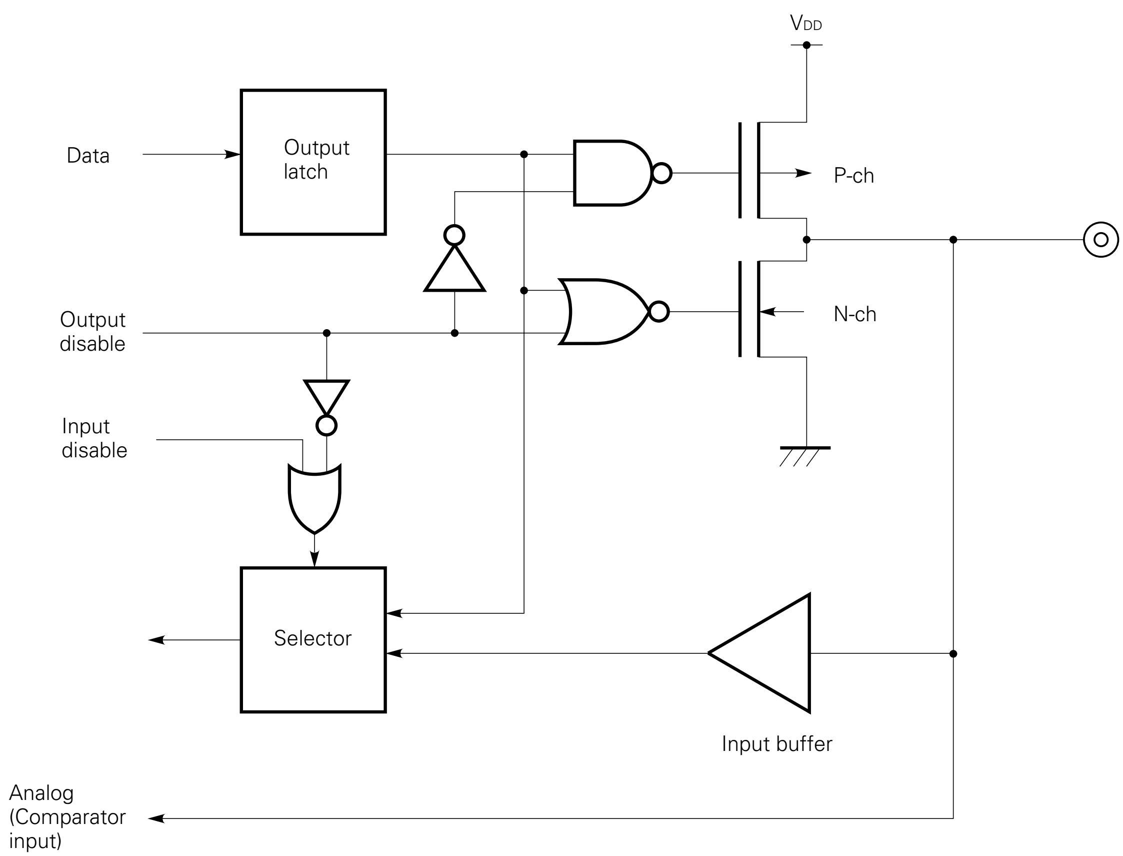
1.3 PIN EQUIVALENT CIRCUIT

Below are simplified diagrams of the input/output circuits for each pin.

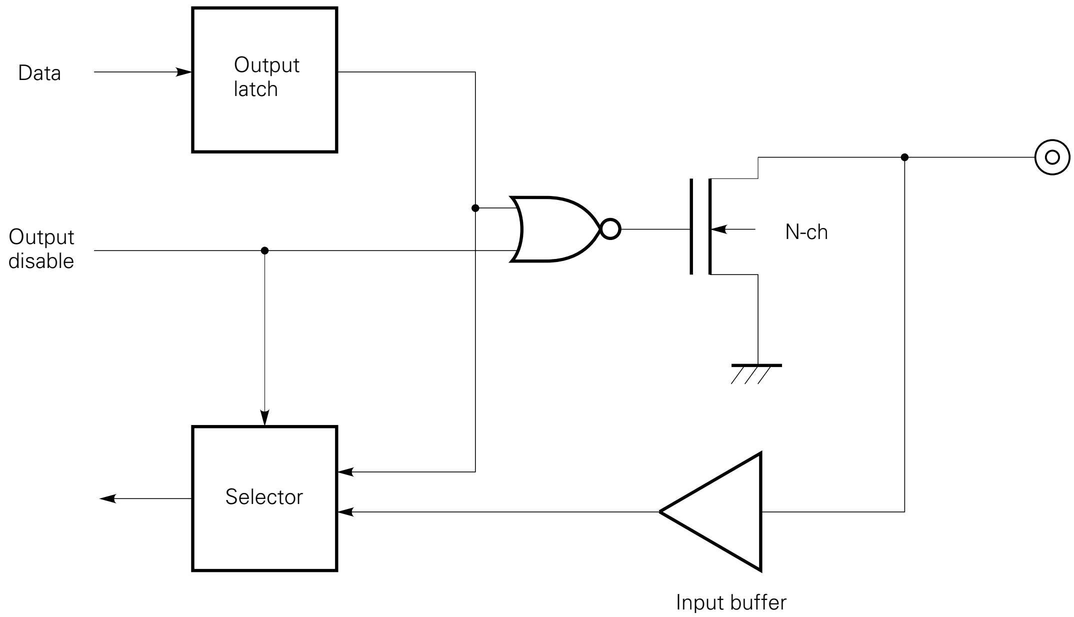
(1) P0A$_0$ to P0A$_3$, P0B$_0$ to P0B$_3$



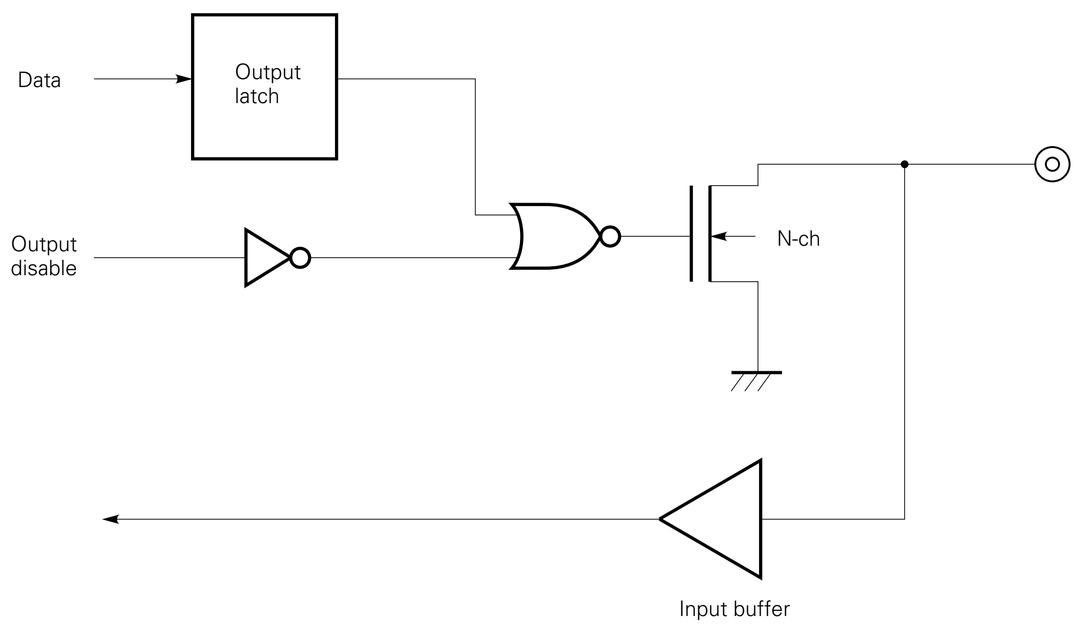
(2) P0C$_0$/Cin$_0$ to P0C$_3$/Cin$_3$



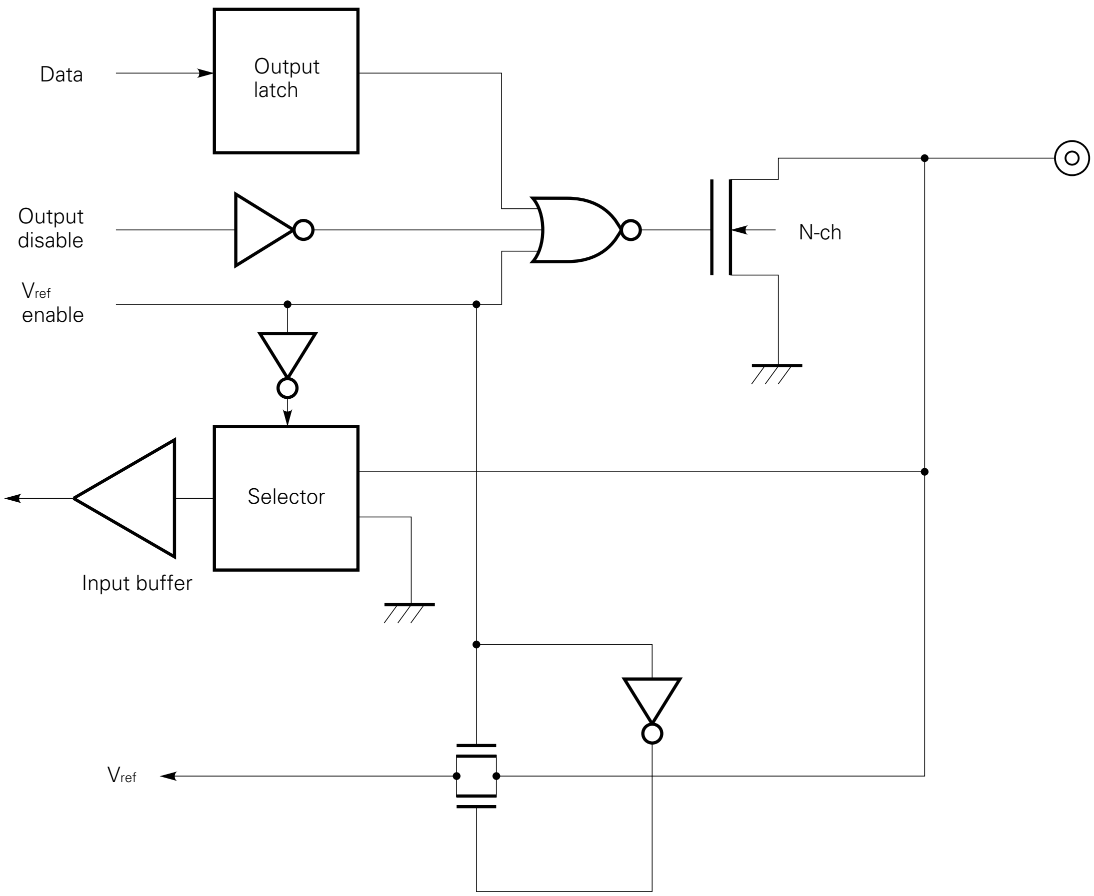
(3) P0D0 to P0D3



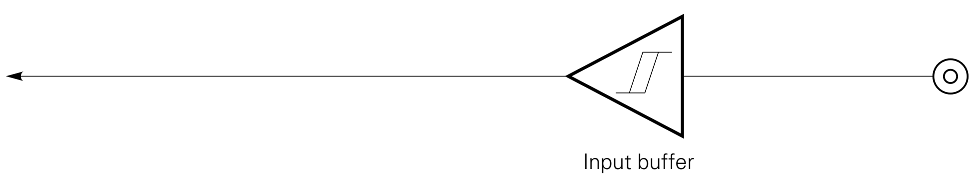
(4) P0E0



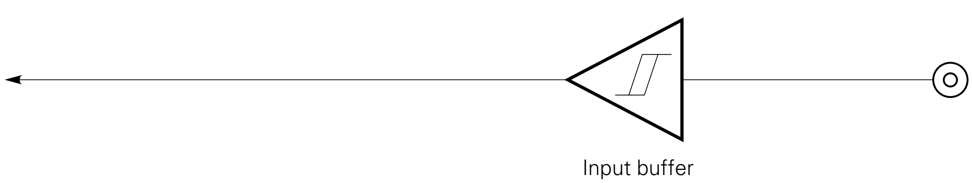
(5) P0E$_1$/V$_{ef}$



(6) INT



(7) $\overline{\text{RESET}}$



★ 1.4 HANDLING UNUSED PINS

In normal operation mode, connect unused pins as follows:

Table 1-1 Handling Unused Pins

Pin			Recommended conditions and handling	
			Internal	External
Port	Input mode	P0A, P0B, P0C, P0D, P0E	—	Connect to V_{DD} or ground through resistors for each pin.Note 1
	Output mode	P0A, P0B, P0C (CMOS ports)	—	Leave open.
		P0D, P0E (N-ch open-drain port)	Outputs low level to pins.	
External interrupt (INT)Note 2			—	Connect directly to ground.
$\overline{\text{RESET}}$Note 3 (when only the built-in power-on/ power-down reset function is used)			—	Connect directly to V_{DD}.

Notes 1. When a pin is pulled up to V_{DD} (connected to V_{DD} through a resistor) or pulled down to ground (connected to ground through a resistor) outside the chip, take the driving capacity and maximum current consumption of a port into consideration. When using high-resistance pull-up or pull-down resistors, apply appropriate countermeasures to ensure that noise is not attracted by the resistors. Although the optimum pull-up or pull-down resistor varies with the application circuit, in general, a resistor of 10 to 100 kilohms is suitable.

2. Since the INT pin is also used for setting the test mode, connect it directly to ground when the pin is not used.

3. When designing an application circuit which requires high reliability, be sure to design a circuit to which an external $\overline{\text{RESET}}$ signal can be input. Since the $\overline{\text{RESET}}$ pin is also used for setting the test mode, connect it to V_{DD} directly when not used.

Caution To fix the I/O mode and output level of a pin, it is recommended that they should be specified repeatedly within a loop in a program.

1.5 NOTES ON USE OF THE $\overline{\text{RESET}}$ AND INT PINS (FOR NORMAL OPERATION MODE ONLY)

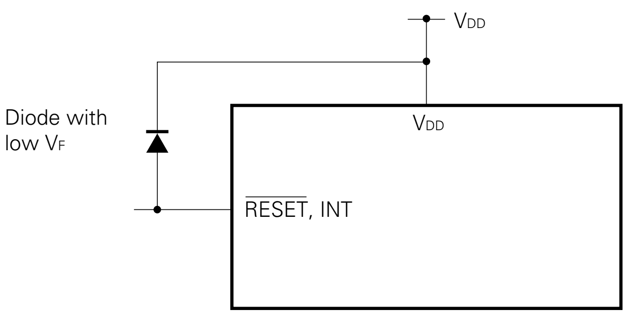
The $\overline{\text{RESET}}$ and INT pins have the test mode selecting function for testing the internal operation of the μPD17P133 (IC test), besides the functions shown in **Section 1.1.**

Applying a voltage exceeding V_{DD} to the $\overline{\text{RESET}}$ and/or INT pin causes the μPD17P133 to enter the test mode. When noise exceeding V_{DD} comes in during normal operation, the device is switched to the test mode.

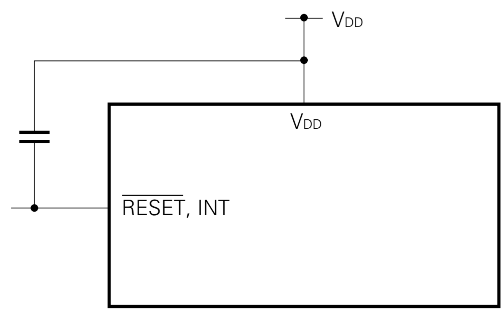
For example, if the wiring from the $\overline{\text{RESET}}$ or INT pin is too long, noise may be induced on the wiring, causing this mode switching.

When installing the wiring, lay the wiring in such a way that noise is suppressed as much as possible. If noise yet arises, use an external part to suppress it as shown below.

- **Connect a diode with low V_F between the pin and V_{DD}.**



- **Connect a capacitor between the pin and V_{DD}.**



2. DIFFERENCES BETWEEN THE μPD17P133, μPD17121, AND μPD17133

The μPD17P133 is a one-time PROM version of the μPD17133, in which the internal masked ROM is replaced with a one-time PROM.

Table 2-1 lists the differences between the μPD17P133, μPD17121, and μPD17133.

The μPD17P133 has the same CPU functions and internal peripheral hardwares as those of μPD17121 and μPD17133 except for its program memory, program memory size, data memory size, operating frequency range, electrical characteristics, and mask option. The μPD17P133 can be used for evaluation of programs during μPD17121/μPD17133 system development.

Table 2-1 Differences between the μPD17P133, μPD17121, and μPD17133

Item	μPD17P133	μPD17121	μPD17133
Program memory (ROM)	One-time PROM	Masked ROM	
	2K bytes (1024 × 16 bits) (0000H - 03FFH)	1.5K bytes (768 × 16 bits) (0000H - 02FFH)	2K bytes (1024 × 16 bits) (0000H - 03FFH)
Data memory (RAM)	111 × 4 bits	64 × 4 bits	111 × 4 bits
Pull-up resistors of P0D, P0E, and $\overline{RESET}$ pins	Not provided	Mask option	
V_{PP} and operation mode selection pins	Provided	Not provided	
Comparator	Provided	Not provided	Provided
Withstand voltage of the $P0E_1$ pin Note	V_{DD}	9 V	V_{DD}
Quality grade	Standard		• Standard (μPD17133) • Special (μPD17133(A))

Note The $P0E_1$ pin of the μPD17133 or μPD17P133 is an N-ch open-drain I/O pin. However, the pin cannot be used as an intermediate-withstand-voltage port pin because this pin is also used as the V_{ref} pin.

Caution Although a PROM product is highly compatible with a masked ROM product in respect of functions, they differ in internal ROM circuits and part of electrical characteristics.
Before changing the PROM product to the masked ROM product in an application system, evaluate the system carefully using the masked ROM product.

3. WRITING TO AND VERIFYING ONE-TIME PROM (PROGRAM MEMORY)

The μPD17P133's internal program memory consists of a 1024 × 16 bit one-time PROM.

Writing to the one-time PROM or verifying the contents of the PROM is accomplished using the pins shown in the table below. Note that address inputs are not used; instead, the address is updated using the clock input from the CLK pin.

Table 3-1 Pins Used When Writing to Program Memory or Verifying Its Contents

Pin name	Function
V_{PP}	Voltage (+12.5 V) is applied to this pin when writing to program memory or verifying its contents.
V_{DD}	Power supply pin. +6 V is applied to this pin when writing to program memory or verifying its contents.
CLK	Input pin for address update clocks used when writing to program memory or verifying its contents. Input of four pulses to this pin updates the address of the program memory.
MD_0 - MD_3	Input pins that select an operation mode when writing to program memory or verifying its contents
D_0 - D_7	Input/output pins for 8-bit data used when writing to program memory or verifying its contents

3.1 PROGRAM MEMORY WRITE/VERIFY MODES

If +6 V is applied to the V_{DD} pin and +12.5 V is applied to the V_{PP} pin after a certain duration of reset status (V_{DD} = 5 V, $\overline{RESET}$ = 0 V), the μPD17P133 enters program memory write/verify mode. A specific operating mode is then selected by setting the MD_0 through MD_3 pins as follows. Connect each pin not listed in Table 3-1 to ground through a pull-down resistor. (However, the X_{OUT} pin must be left open.)

For details, see **PIN CONFIGURATION (2)**.

Table 3-2 Specification of Operating Modes

Operating mode specification						Operating mode
V_{PP}	V_{DD}	MD_0	MD_1	MD_2	MD_3	
+12.5 V	+6 V	H	L	H	L	Program memory address clear mode
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	×	H	H	Program inhibit mode

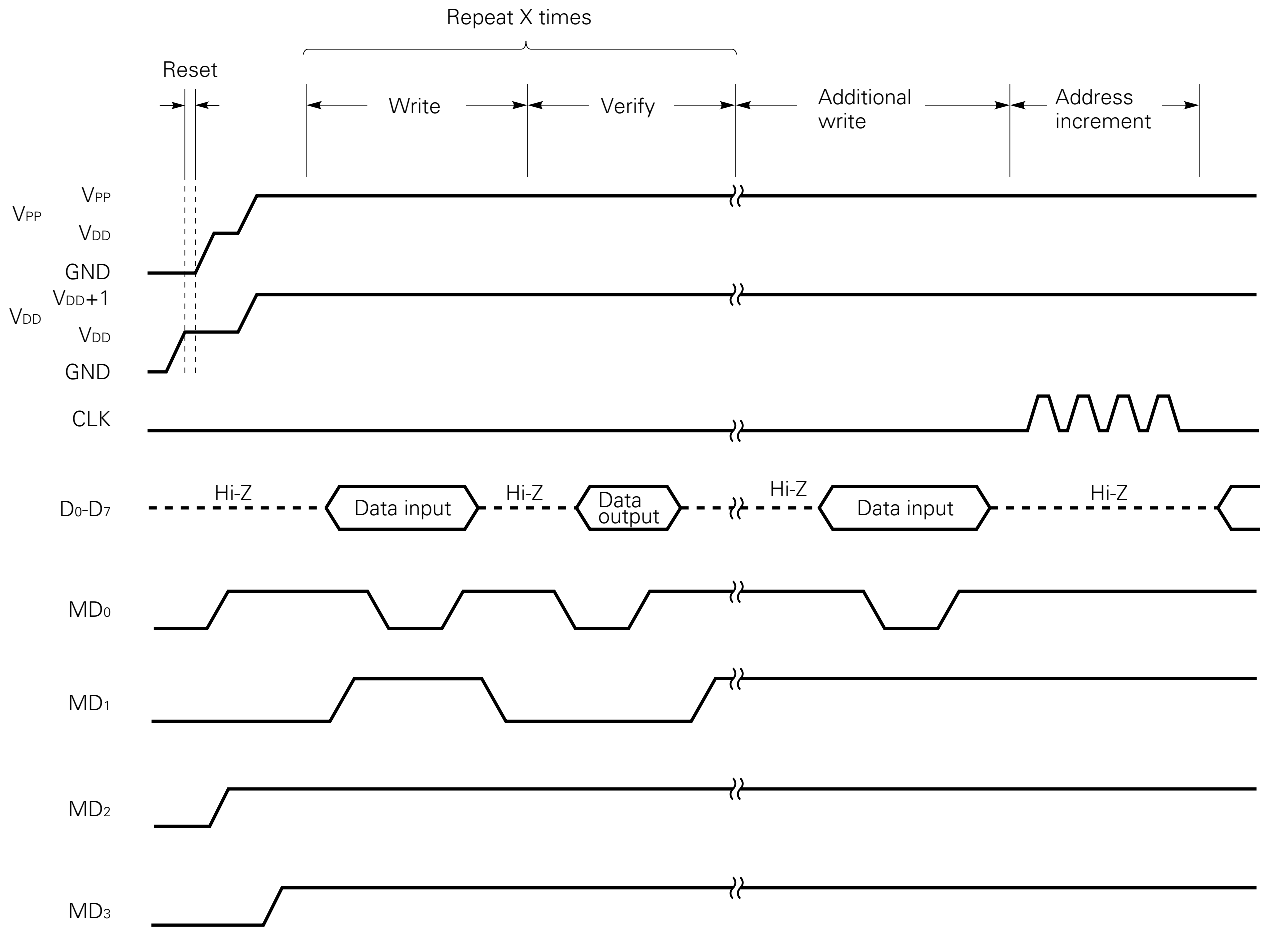
Remark ×: Don't care. L (low) or H (high)

3.2 WRITING TO PROGRAM MEMORY

The procedure for writing to program memory is described below; high-speed write is possible.

(1) Pull low the levels of all unused pins to GND by means of resistors (the X_{OUT} pin is left open). Bring CLK to low level.
(2) Apply 5 V to V_{DD} and bring V_{PP} to low level.
(3) Wait 10 μs. Then apply 5 V to V_{PP}.
(4) Set the mode selection pins to program memory address clear mode.
(5) Apply 6 V to V_{DD} and 12.5 V to V_{PP}.
(6) Select program inhibit mode.
(7) Write data in 1-ms write mode.
(8) Select program inhibit mode.
(9) Select verify mode. If the write operation is found successful, proceed to step (10). If the operation is found unsuccessful, repeat steps (7) to (9).
(10) Perform additional write for X (number of repetitions of steps (7) to (9)) × 1 ms.
(11) Select program inhibit mode.
(12) Increment the program memory address by one on reception of four pulses on the CLK pin.
(13) Repeat steps (7) to (12) until the last address is reached.
(14) Select program memory address clear mode.
(15) Apply 5 V to the V_{DD} and V_{PP} pins.
(16) Turn power off.

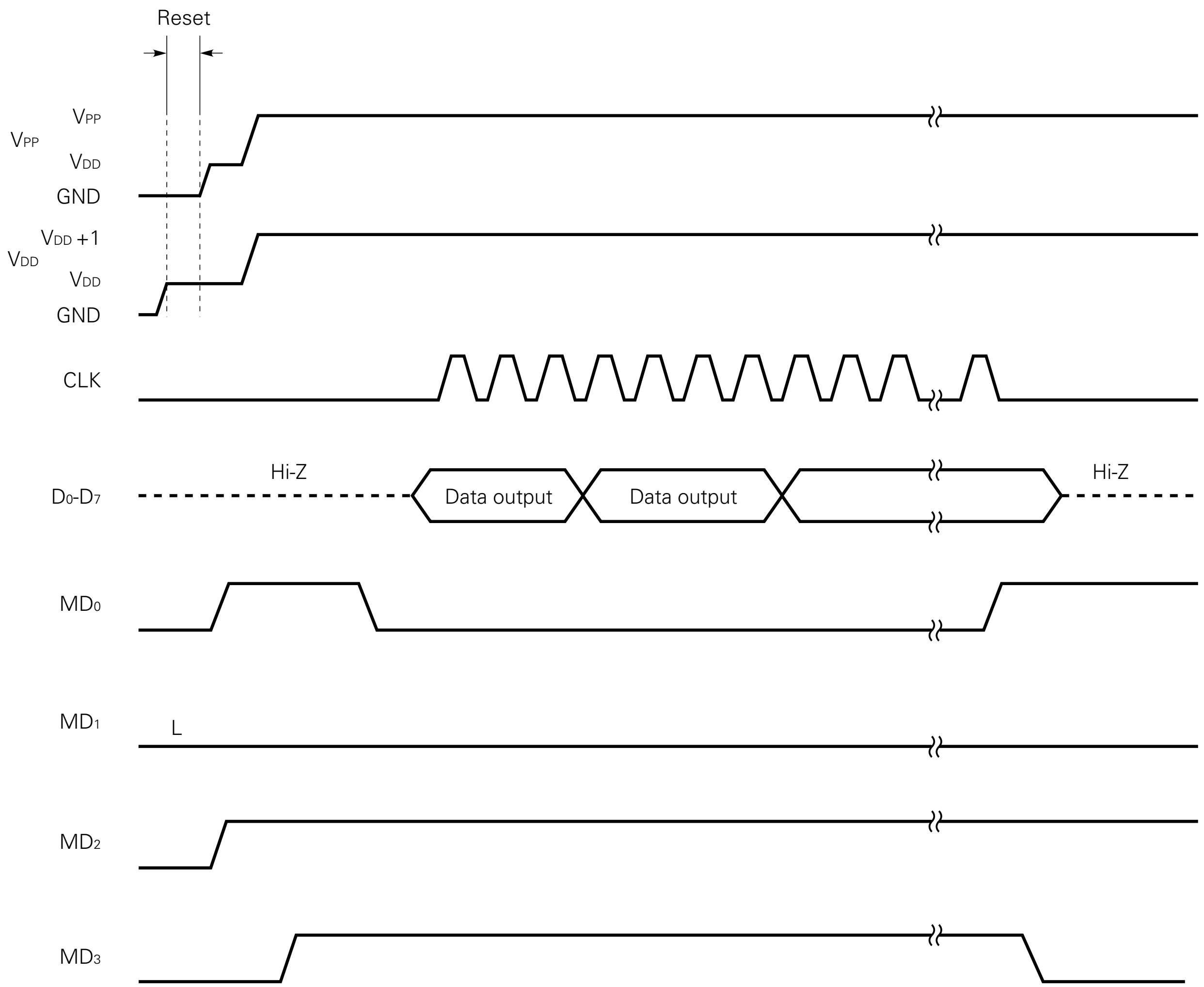
A timing chart for program memory writing steps (2) to (12) is shown below.



3.3 READING PROGRAM MEMORY

(1) Pull low the levels of all unused pins to GND by means of resistors (the X_{OUT} pin is left open). Bring CLK to low level.
(2) Apply 5 V to V_{DD} and bring V_{PP} to low level.
(3) Wait 10 μs. Then apply 5 V to V_{PP}.
(4) Set the mode selection pins to program memory address clear mode.
(5) Apply 6 V to V_{DD} and 12.5 V to V_{PP}.
(6) Select program inhibit mode.
(7) Select verify mode. Data is output sequentially one address at a time for every four input clock pulses on the CLK.
(8) Select program inhibit mode.
(9) Select program memory address clear mode.
(10) Apply 5 V to the V_{DD} and V_{PP} pins.
(11) Turn power off.

A timing chart for program memory reading steps (2) to (9) is shown below.



★ 4. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Parameter	Symbol	Conditions		Rated value	Unit
Power supply voltage	V_{DD}			−0.3 to +7.0	V
Input voltage	V_I	P0A, P0B, P0C, P0E1 Note, INT, RESET		−0.3 to V_{DD} + 0.3	V
		P0D, P0E0		−0.3 to +10.0	V
Output voltage	V_O	P0A, P0B, P0C, P0E1 Note		−0.3 to V_{DD} + 0.3	V
		P0D, P0E0		−0.3 to +10.0	V
High-level output current	I_{OH}	Each of P0A, P0B, and P0C		−5	mA
		Total of all output pins		−20	mA
Low-level output current	I_{OL}	Each of P0A, P0B, and P0C		5	mA
		Each of P0D and P0E		30	mA
		Total of P0A, P0B, and P0C output pins		20	mA
		Total of P0D and P0E output pins		60	mA
		Total of all output pins		80	mA
Operating ambient temperature	T_A			−40 to +85	°C
Storage temperature	T_{stg}			−65 to +150	°C
Allowable dissipation	P_d	T_A = 85 °C	Plastic shrink DIP	155	mW
			Plastic SOP	95	mW

Note The P0E1 N-ch open-drain input/output pin cannot be used as an intermediate-withstand-voltage port pin.

Caution Absolute maximum ratings are rated values beyond which some physical damages may be caused to the product; if any of the parameters in the table above exceeds its rated value even for a moment, the quality of the product may deteriorate. Be sure to use the product within the rated values.

RECOMMENDED POWER VOLTAGE RANGE (T_A = −40 to +85 °C)

Parameter	Conditions	Min.	Typ.	Max.	Unit
CPU Note	Oscillator frequency: f_X = 400 kHz to 4 MHz	2.7		5.5	V
	Oscillator frequency: f_X = 400 kHz to 8 MHz	4.5		5.5	V
Power-on/power-down reset circuit	Rising time of the power voltage (V_{DD} = 0 → 2.7 V): 4096t_{CY} or less (f_X = 400 kHz to 4 MHz)	4.5		5.5	V

Note Excluding the power-on/power-down reset circuit

Remark t_{CY} = 16/f_X (f_X: frequency of the system clock oscillator)

DC CHARACTERISTICS (V_{DD} = 2.7 to 5.5 V, T_A = −40 to +85 °C)

Parameter	Symbol	Conditions			Min.	Typ.	Max.	Unit
High-level input voltage	V_{IH1}	P0A, P0B, P0C, P0D, P0E			0.7V_{DD}		V_{DD}	V
	V_{IH2}	$\overline{RESET}$, $\overline{SCK}$, SI, INT			0.8V_{DD}		V_{DD}	V
Low-level input voltage	V_{IL1}	P0A, P0B, P0C			0		0.3V_{DD}	V
	V_{IL2}	P0D, P0E, $\overline{RESET}$, $\overline{SCK}$, SI, INT			0		0.2V_{DD}	V
High-level output voltage	V_{OH}	P0A, P0B, P0C	V_{DD} = 4.5 to 5.5 V, I_{OH} = −1.0 mA		V_{DD} − 0.3			V
			V_{DD} = 2.7 to 4.5 V, I_{OH} = −0.5 mA		V_{DD} − 0.3			V
Low-level output voltage	V_{OL1}	P0A, P0B, P0C, P0D, P0E	V_{DD} = 4.5 to 5.5 V, I_{OL} = 1.0 mA				0.3	V
			V_{DD} = 2.7 to 4.5 V, I_{OL} = 0.5 mA				0.3	V
	V_{OL2}	P0D, P0E	V_{DD} = 4.5 to 5.5 V, I_{OL} = 15 mA				1.0	V
			V_{DD} = 2.7 to 4.5 V, I_{OL} = 15 mA				2.0	V
High-level input leakage current	I_{LIH}	P0A, P0B, P0C, P0D, P0E, V_{IN} = V_{DD}					3	μA
Low-level input leakage current	I_{LIL}	P0A, P0B, P0C, P0D, P0E, V_{IN} = 0 V					−3	μA
High-level output leakage current	I_{LOH}	P0A, P0B, P0C, P0D, P0E, V_{OUT} = V_{DD}					3	μA
Low-level output leakage current	I_{LOL}	P0A, P0B, P0C, P0D, P0E, V_{OUT} = 0 V					−3	μA
Power supply current**Note**	I_{DD1}	Operating mode	f_X = 8.0 MHz, V_{DD} = 5 V ±10 %			5.0	8.0	mA
			f_X = 4.0 MHz, V_{DD} = 5 V ±10 %			3.0	5.0	mA
			f_X = 2.0 MHz, V_{DD} = 3 V ±10 %			1.0	2.5	mA
			f_X = 455 kHz	V_{DD} = 5 V ±10 %		2.0	4.5	mA
				V_{DD} = 3 V ±10 %		0.7	2.2	mA
	I_{DD2}	HALT mode	f_X = 8.0 MHz, V_{DD} = 5 V ±10 %			3.5	5.0	mA
			f_X = 4.0 MHz, V_{DD} = 5 V ±10 %			2.5	3.5	mA
			f_X = 2.0 MHz, V_{DD} = 3 V ±10 %			0.8	2.0	mA
			f_X = 455 kHz	V_{DD} = 5 V ±10 %		1.8	3.5	mA
				V_{DD} = 3 V ±10 %		0.6	1.9	mA
	I_{DD3}	STOP mode	V_{DD} = 5 V ±10 %			3.0	10	μA
			V_{DD} = 3 V ±10 %			2.0	10	μA

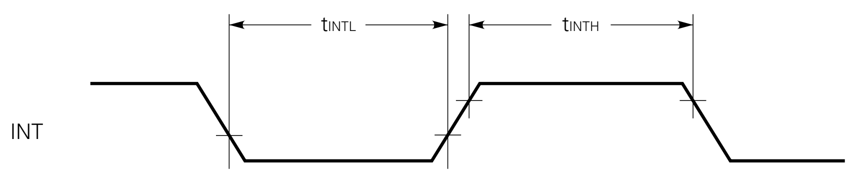
Note This current excludes the current which flows through the comparator.

AC CHARACTERISTICS (V_{DD} = 2.7 to 5.5 V, T_A = −40 to +85 °C)

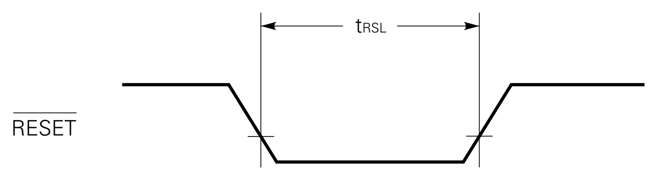
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
CPU clock cycle time (instruction execution time)	t_{CY}	V_{DD} = 4.5 to 5.5 V	1.9		41	μs
			3.9		41	μs
INT high/low level width (external interrupt input)	t_{INTH}, t_{INTL}	V_{DD} = 4.5 to 5.5 V	10			μs
			50			μs
$\overline{\text{RESET}}$ low level width	t_{RSL}	V_{DD} = 4.5 to 5.5 V	10			μs
			50			μs

Remark t_{CY} = 16/f_X (f_X: frequency of system clock oscillator)

Interrupt Input Timing



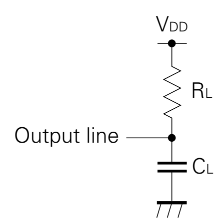
$\overline{\text{RESET}}$ Input Timing



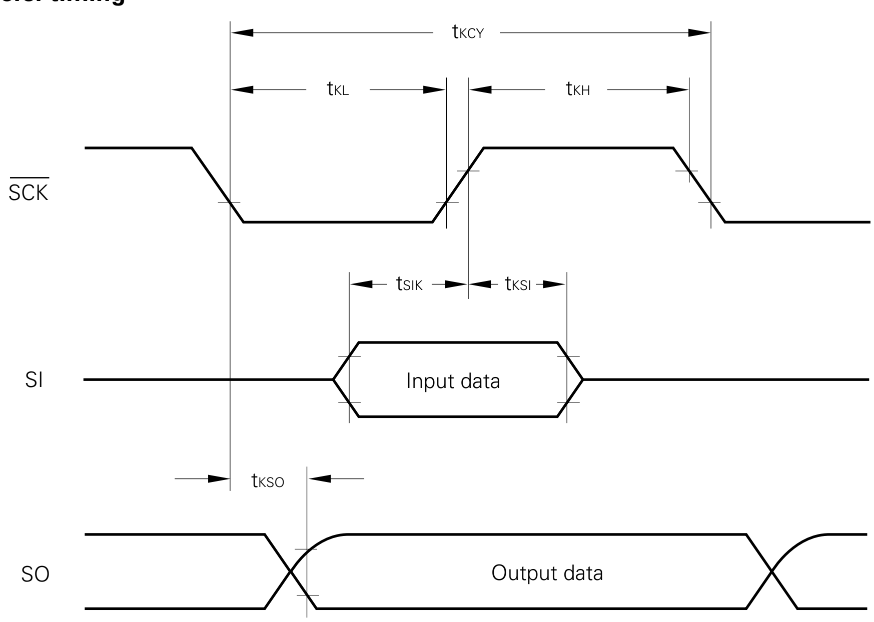
SERIAL TRANSFER OPERATION (V_{DD} = 2.7 to 5.5 V, T_A = –40 to +85 °C)

Parameter	Symbol		Conditions		Min.	Typ.	Max.	Unit
$\overline{SCK}$ cycle time	t_{KCY}	Input	V_{DD} = 4.5 to 5.5 V		2.0			μs
		Input			10			μs
		Output	R_L = 1 kΩ, C_L = 100 pF	V_{DD} = 4.5 to 5.5 V	2.0			μs
		Output			16			μs
$\overline{SCK}$ high/low level width	t_{KH}, t_{KL}	Input	V_{DD} = 4.5 to 5.5 V		1.0			μs
		Input			5.0			μs
		Output	R_L = 1 kΩ, C_L = 100 pF	V_{DD} = 4.5 to 5.5 V	t_{KCY}/2–0.6			μs
		Output			t_{KCY}/2–1.2			μs
SI setup time (with respect to $\overline{SCK}$↑)	t_{SIK}				100			ns
SI hold time (with respect to $\overline{SCK}$↑)	t_{KSI}				100			ns
Delay from $\overline{SCK}$↓ to SO	t_{KSO}		R_L = 1 kΩ, C_L = 100 pF	V_{DD} = 4.5 to 5.5 V			0.8	μs
							1.4	μs

Remark R_L and C_L are a resistive load and a capacitive load for the output line.



Serial transfer timing



POWER-ON/POWER-DOWN RESET CIRCUIT CHARACTERISTICS (T_A = –40 to +85 °C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power voltage rise time when power-on reset is valid	t_{POR}	V_{DD} = 0 → 2.7 V Rising must start at 0 V. f_X = 400 kHz to 4 MHz			4096t_{CY}	μs
Voltage for power-down reset circuit	V_{PDR}	When PDRESEN = 1		3.5	4.5	V

Remark t_{CY} = 16/f_X (f_X: frequency of the system clock oscillator)

COMPARATOR CHARACTERISTICS (V_{DD} = 2.7 to 5.5 V, T_A = –40 to +85 °C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Comparator input voltage range	V_{AIN}	Cin_0 - Cin_3, V_{ref}	0		V_{DD}	V
Resolution**Note 1**		V_{DD} = 4.5 to 5.5 V		10	50	mV
					100	mV
Response time		**Note 2**			6t_{CY}	μs

Notes 1. Also applied to the condition that the internal reference voltage is used.

2. Time required for storing the comparison result in CMPRSLT after execution of the comparator start instruction (execution time not included). (12 μs, when f_X = 8 MHz)

Remark t_{CY} = 16/f_X (f_X: frequency of the system clock oscillator)

SYSTEM CLOCK OSCILLATOR CHARACTERISTICS (V_{DD} = 2.7 to 5.5 V, T_A = –40 to +85 °C)

Resonator	Parameter	Conditions	Min.	Typ.	Max.	Unit
Ceramic resonator	Oscillation frequency (f_X)		0.39		4.08	MHz
		V_{DD} = 4.5 to 5.5 V	0.39		8.16	MHz

DC PROGRAMMING CHARACTERISTICS (V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.5 V, T_A = 25 °C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input voltage high	V_{IH1}	Except CLK	0.7V_{DD}		V_{DD}	V
	V_{IH2}	CLK	V_{DD} – 0.5		V_{DD}	V
Input voltage low	V_{IL1}	Except CLK	0		0.3V_{DD}	V
	V_{IL2}	CLK	0		0.4	V
Input leakage current	I_{LI}	V_{IN} = V_{IL} or V_{IH}			10	μA
Output voltage high	V_{OH}	I_{OH} = –1 mA	V_{DD} –1.0			V
Output voltage low	V_{OL}	I_{OL} = 1.6 mA			0.4	V
V_{DD} power supply current	I_{DD}				30	mA
V_{PP} power supply current	I_{PP}	MD0 = V_{IL}, MD1 = V_{IH}			30	mA

Cautions 1. V_{PP} must be under +13.5 V including overshoot.

2. V_{DD} must be applied before V_{PP} on and must be off after V_{PP} off.

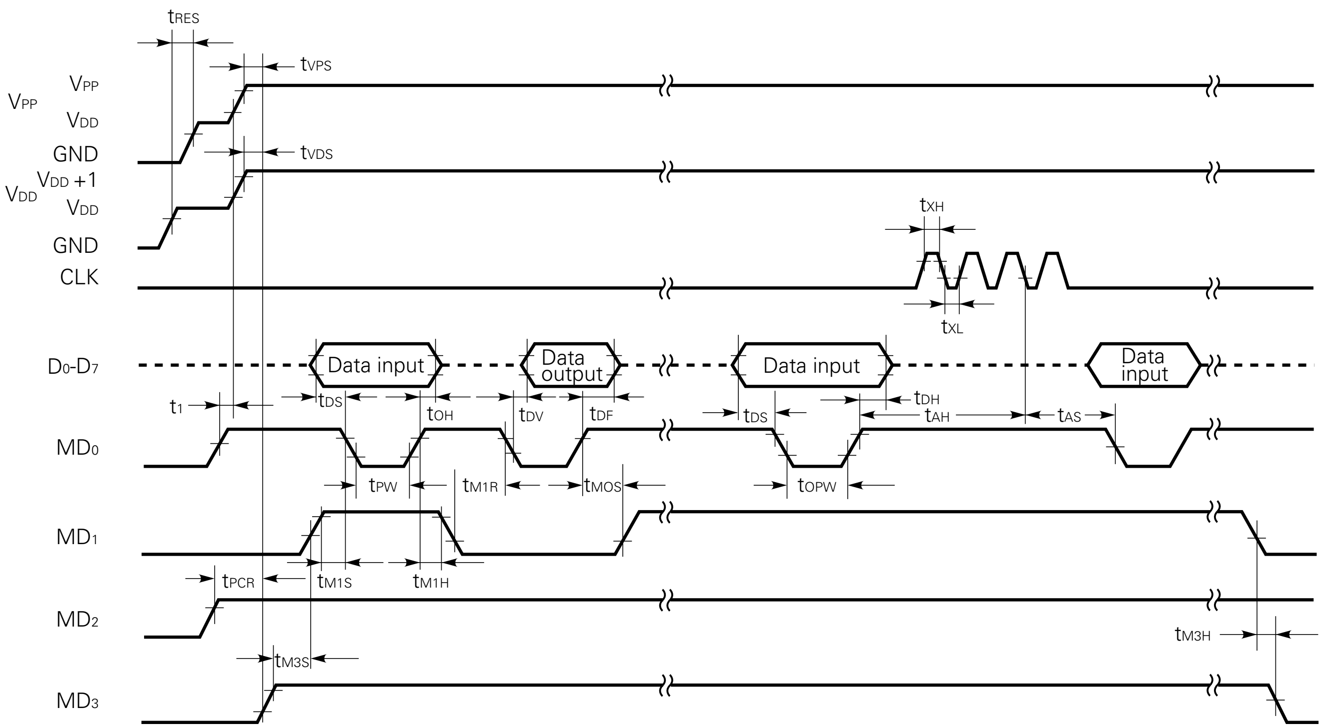
AC PROGRAMMING CHARACTERISTICS (V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.5 V, T_A = 25 °C)

Parameter	Symbol	Note 1	Conditions	Min.	Typ.	Max.	Unit
Address setup time Note 2 to MD0↓	t_{AS}	t_{AS}		2			μs
MD1 setup time to MD0↓	t_{M1S}	t_{OES}		2			μs
Data setup time to MD0↓	t_{DS}	t_{DS}		2			μs
Address hold time Note 2 to MD0↑	t_{AH}	t_{AH}		2			μs
Data hold time to MD0↑	t_{DH}	t_{DH}		2			μs
Delay from MD0↑ to data output float	t_{DF}	t_{DF}		0		130	ns
V_{PP} setup time to MD3↑	t_{VPS}	t_{VPS}		2			μs
V_{DD} setup time to MD3↑	t_{VDS}	t_{VCS}		2			μs
Initial program pulse width	t_{PW}	t_{PW}		0.95	1.0	1.05	ms
Additional program pulse width	t_{OPW}	t_{OPW}		0.95		21.0	ms
MD0 setup time to MD1↑	t_{MOS}	t_{CES}		2			μs
Delay from MD0↓ to data output	t_{DV}	t_{DV}	MD0 = MD1 = V_{IL}			1	μs
MD1 hold time to MD0↑	t_{M1H}	t_{OEH}	$t_{M1H} + t_{M1R} \geq 50$ μs	2			μs
MD1 recovery time to MD0↓	t_{M1R}	t_{OR}		2			μs
Program counter reset time	t_{PCR}	–		10			μs
CLK input high, low level range	t_{XH}, t_{XL}	–		0.125			μs
CLK input frequency	f_X	–				2	MHz
Initial mode set time	t_I	–		2			μs
MD3 setup time to MD1↑	t_{M3S}	–		2			μs
MD3 hold time to MD1↓	t_{M3H}	–		2			μs
MD3 setup time to MD0↓	t_{M3SR}	–	Read program memory	2			μs
Delay from address Note 2 to data output	t_{DAD}	t_{ACC}	Read program memory			2	μs
Hold time from address Note 2 to data output	t_{HAD}	t_{OH}	Read program memory	0		130	ns
MD3 hold time to MD0↑	t_{M3HR}	–	Read program memory	2			μs
Delay from MD3↓ to data output float	t_{DFR}	–	Read program memory			2	μs
Reset setup time	t_{RES}			10			μs

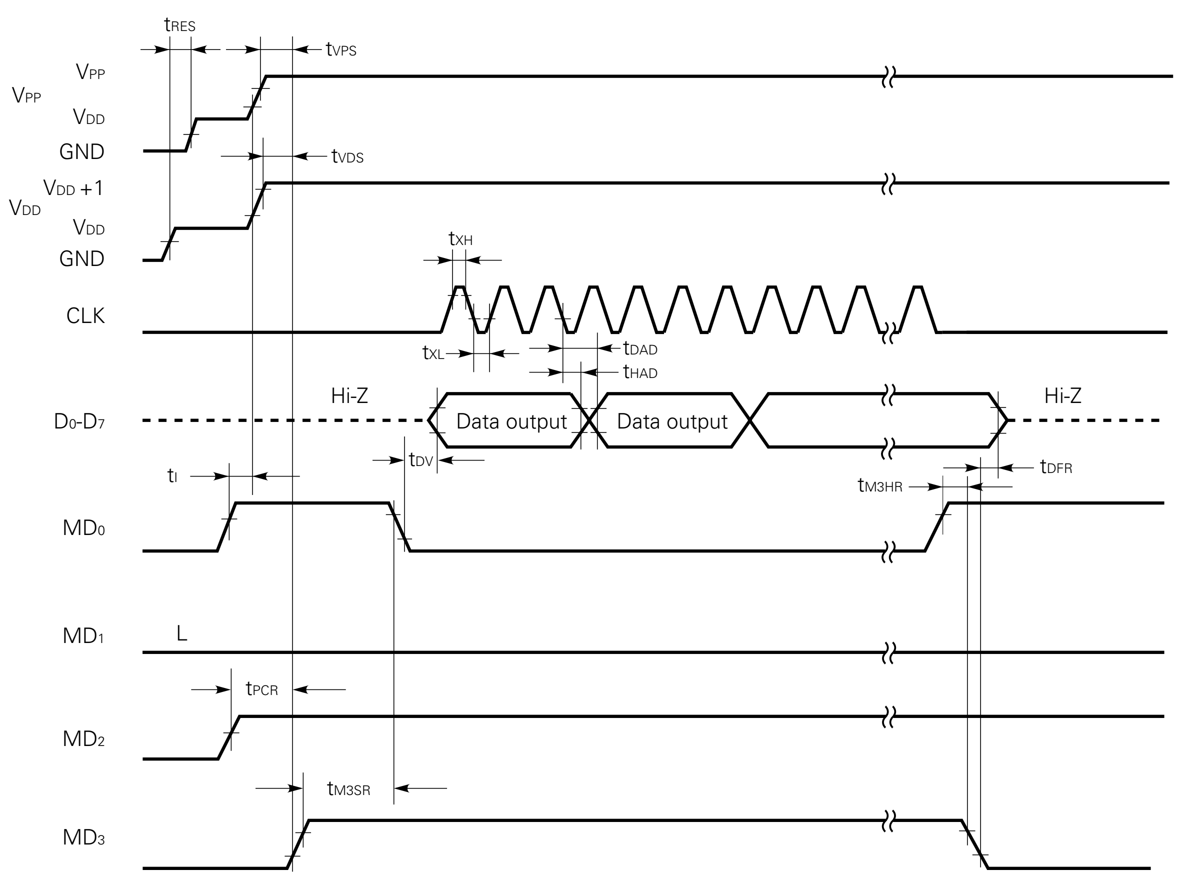
Notes 1. Corresponding symbol for μPD27C256A (used for maintenance)

2. The internal address is incremented by one at the falling edge of the third clock (CLK) input.

Write program memory timing



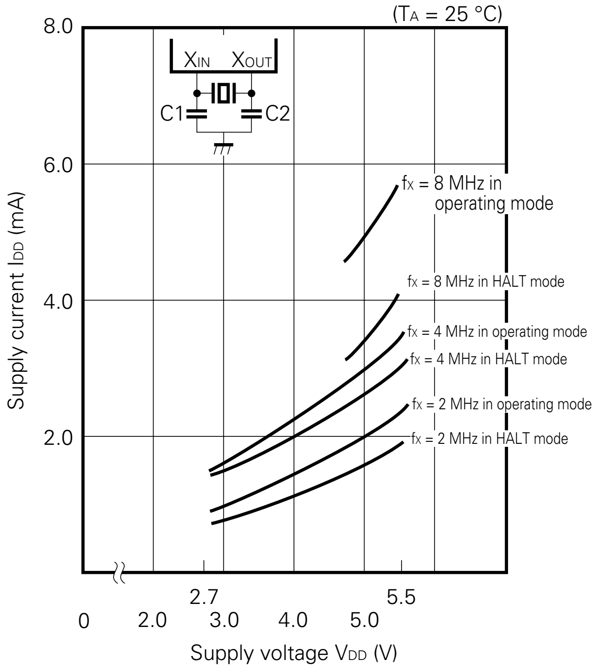
Read program memory timing



Remark The dashed line indicates high-impedance.

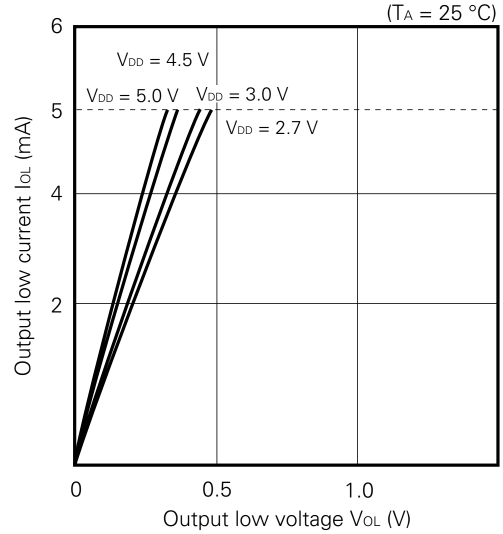
5. CHARACTERISTIC CURVES (FOR REFERENCE)

I_{DD} vs V_{DD}



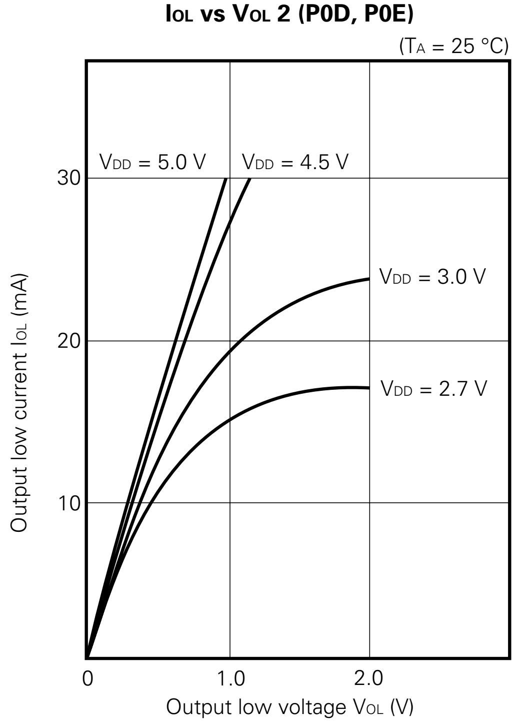
Caution The absolute maximum rating of the current is 5 mA per pin.

I_{OL} vs V_{OL} 1 (P0A, P0B, P0C)



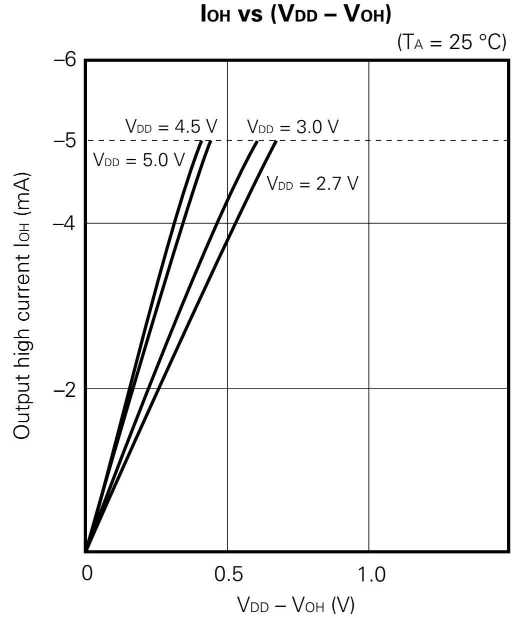
Caution The absolute maximum rating of the current is 5 mA per pin.

I_{OL} vs V_{OL} 2 (P0D, P0E)



Caution The absolute maximum rating of the current is 30 mA per pin. The input voltage or output voltage of the P0E$_1$ pin must not be higher than V_{DD} + 0.3 V.

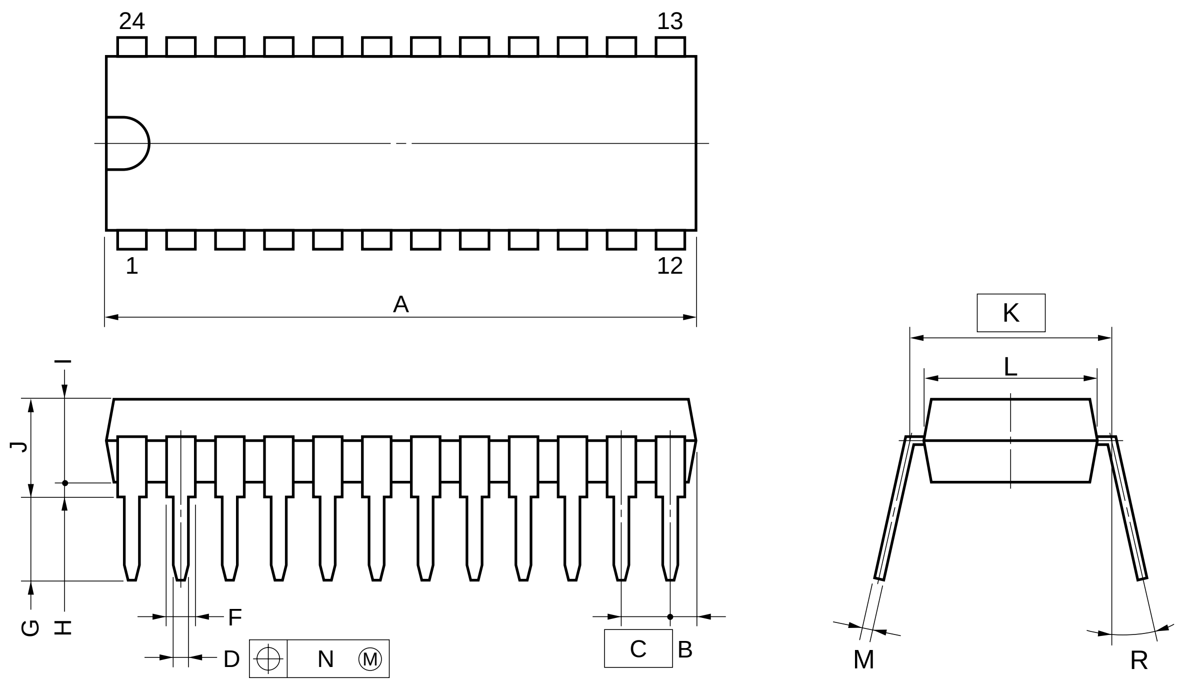
I_{OH} vs (V_{DD} – V_{OH})



Caution The absolute maximum rating of the current is –5 mA per pin.

6. PACKAGE DRAWINGS

24 PIN PLASTIC SHRINK DIP (300 mil)



NOTE

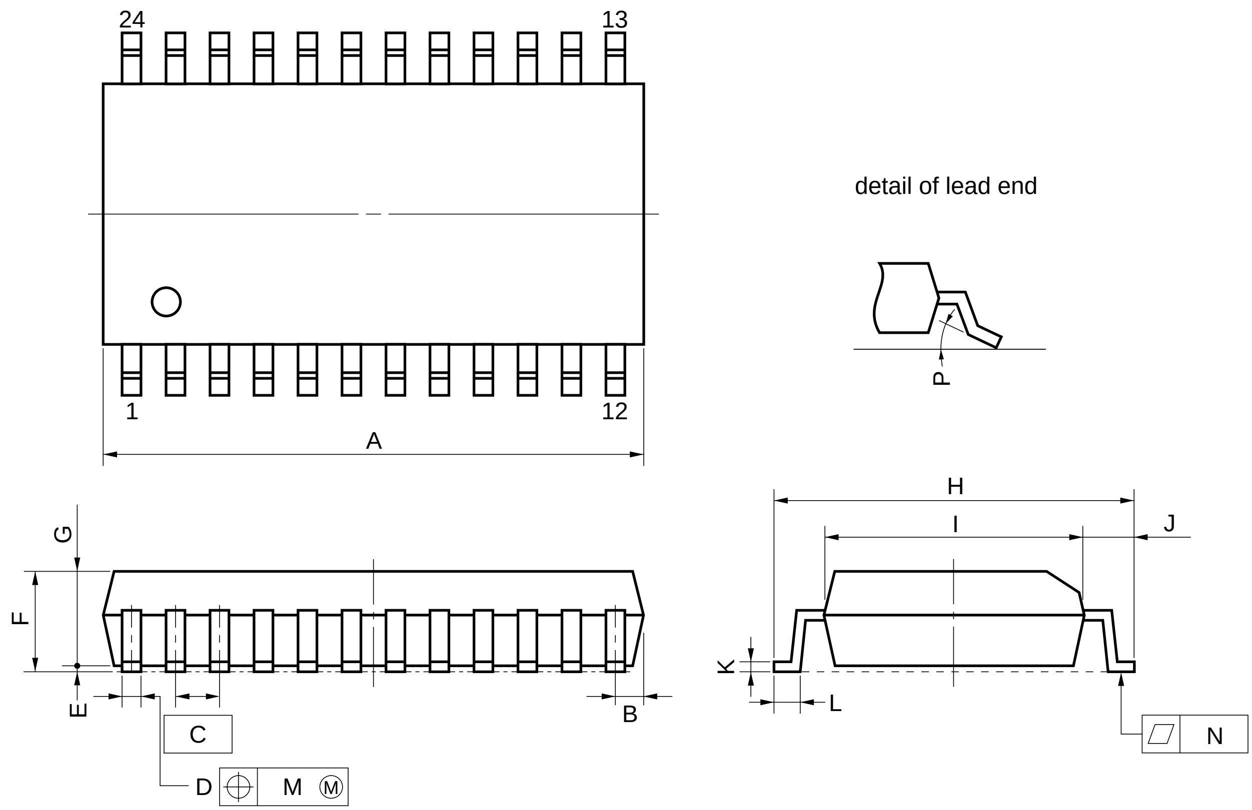
1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	23.12 MAX.	0.911 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50±0.10	$0.020^{+0.004}_{-0.005}$
F	0.85 MIN.	0.033 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.5	0.256
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

S24C-70-300B-1

24 PIN PLASTIC SOP (375 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	15.54 MAX.	0.612 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1±0.1	0.004±0.004
F	2.9 MAX.	0.115 MAX.
G	2.50	0.098
H	10.3±0.3	$0.406^{+0.012}_{-0.013}$
I	7.2	0.283
J	1.6	0.063
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	0.12	0.005
N	0.15	0.006
P	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$

P24GM-50-375B-3

7. RECOMMENDED SOLDERING CONDITIONS ★

The conditions listed below shall be met when soldering the μPD17P133.

For details of the recommended soldering conditions, refer to our document *SMD Surface Mount Technology Manual* (IEI-1207).

Please consult with our sales offices in case any other soldering process is used, or in case soldering is done under different conditions.

Table 7-1 Soldering Conditions for Surface-Mount Devices

μPD17P133GT: 24-pin plastic SOP (375 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 235 °C Reflow time: 30 seconds or less (at 210 °C or more) Maximum allowable number of reflow processes: 2 Exposure limit: 7 days[Note] (20 hours of pre-baking is required at 125 °C afterward.) <Cautions> (1) Do not start reflow-soldering the device if its temperature is higher than the room temperature because of a previous reflow soldering. (2) Do not use water for flux cleaning before a second reflow soldering.	IR35-207-2
VPS	Peak package's surface temperature: 215 °C Reflow time: 40 seconds or less (at 200 °C or more) Maximum allowable number of reflow processes: 2 Exposure limit: 7 days[Note] (20 hours of pre-baking is required at 125 °C afterward.) <Cautions> (1) Do not start reflow-soldering the device if its temperature is higher than the room temperature because of a previous reflow soldering. (2) Do not use water for flux cleaning before a second reflow soldering.	VP15-207-2
Wave soldering	Temperature in the soldering vessel: 260 °C or less Soldering time: 10 seconds or less Number of soldering process: 1 Preheating temperature: 120 °C max. (measured on the package surface) Exposure limit: 7 days[Note] (20 hours of pre-baking is required at 125 °C afterward.)	WS60-207-1
Partial heating method	Terminal temperature: 300 °C or less Flow time: 3 seconds or less (for each side of device)	—

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: Temperature of 25 °C and maximum relative humidity at 65 % or less

Caution Do not apply more than a single process at once, except for "Partial heating method."

Table 7-2 Soldering Conditions for Through Hole Mount Devices

μPD17P133CS: 24-pin plastic shrink DIP (300 mil)

Soldering process	Soldering conditions
Wave soldering (only for terminals)	Solder temperature: 260 °C or less Flow time: 10 seconds or less
Partial heating method	Terminal temperature: 300 °C or less Flow time: 3 seconds or less (for each terminal)

Caution In wave soldering, apply solder only to the terminals. Care must be taken that jet solder does not come in contact with the main body of the package.

APPENDIX A μPD17120 SUB-SERIES PRODUCTS LIST

Item \ Product name	μPD17120	μPD17132	μPD17P132	μPD17121	μPD17133	μPD17P133
ROM capacity	Masked ROM		One-time PROM	Masked ROM		One-time PROM
	1.5K bytes (768 × 16 bits)	2K bytes (1024 × 16 bits)		1.5K bytes (768 × 16 bits)	2K bytes (1024 × 16 bits)	
RAM capacity	64 × 4 bits	111 × 4 bits		64 × 4 bits	111 × 4 bits	
Number of input/ output port pins	19 (Input/output pins: 18, Sensor input pins (INT pins): 1)					
External interrupt	1 (with sensor input)					
Analog input	None	Comparators (4 channels)		None	Comparators (4 channels)	
Timer	1 channel					
Serial interface	1 channel					
Stack	Five address stacks and one interrupt stack					
Power-on/power-down reset circuit	Built-in (Can be used in an application circuit where V_{DD} is 5 V ±10 %)			Built-in (Can be used in an application circuit where V_{DD} is 5 V ±10 % and f_X = 400 kHz to 4 MHz)		
System clock	RC oscillation			Ceramic oscillation		
Instruction execution time	8 μs at f_{CC} = 2 MHz			2 μs at f_X = 8 MHz		
Standby function	HALT, STOP					
Supply voltage	• V_{DD} = 2.7 to 5.5 V • V_{DD} = 4.5 to 5.5 V (when the power-on/power-down reset function is used)					
Package	• 24-pin plastic shrink DIP (300 mil) • 24-pin plastic SOP (375 mil)					
One-time PROM product	μPD17P132		—	μPD17P133		—

Remark The comparator can be used as a 4-bit A/D converter by software.

APPENDIX B DEVELOPMENT TOOLS

The following support tools are available for developing programs for the μPD17P133.

Hardware

Name	Description
In-circuit emulator IE-17K IE-17K-ET**Note 1** EMU-17K**Note 2**	The IE-17K, IE-17K-ET, and EMU-17K are in-circuit emulators applicable to the 17K series. The IE-17K and IE-17K-ET are connected to the PC-9800 series (host machine) or IBM PC/AT™ through the RS-232-C interface. The EMU-17K is inserted into the extension slot of the PC-9800 series (host machine). Use the system evaluation board (SE board) corresponding to each product together with one of these in-circuit emulators. SIMPLEHOST™, a man machine interface, implements an advanced debug environment. The EMU-17K also enables user to check the contents of the data memory in real time.
SE board (SE-17120)	The SE-17120 is an SE board for the μPD17120 sub-series. It is used solely for evaluating the system. It is also used for debugging in combination with the in-circuit emulator.
Emulation probe (EP-17120CS)	The EP-17120CS is an emulation probe for the 17K series 24-pin shrink DIP (300 mil). Use this emulation probe to connect the SE board to target system.
★ PROM programmer AF-9703**Note 3** AF-9704**Note 3** AF-9705**Note 3** AF-9706**Note 3**	The AF-9703, AF-9704, AF-9705, and AF-9706 are PROM programmers for the μPD17P133. Use one of these PROM programmers with the program adapter, AF-9808M, to write a program into the μPD17P133.
Program adapter (AF-9808M**Note 3**)	The AF-9808M is a socket unit for the μPD17P133CS or μPD17P133GT. It is used with the AF-9703, AF-9704, AF-9705, or AF-9706.

Notes 1. Low-end model, operating on an external power supply

2. The EMU-17K is a product of IC Co., Ltd. Contact IC Co., Ltd. (Tokyo, 03-3447-3793) for details.

3. The AF-9703, AF-9704, AF-9705, AF-9706, and AF-9808M are products of Ando Electric Co., Ltd. Contact Ando Electric Co., Ltd. (Tokyo, 03-3733-1151) for details.

Software

<table>
<tr><th>Name</th><th>Description</th><th>Host machine</th><th colspan="2">OS</th><th>Distribution media</th><th>Part number</th></tr>
<tr><td rowspan="4">17K series assembler (AS17K)</td><td rowspan="4">AS17K is an assembler applicable to the 17K series. In developing μPD17P133 programs, AS17K is used in combination with a device file (AS17133).</td><td rowspan="2">PC-9800 series</td><td colspan="2" rowspan="2">MS-DOS™</td><td>5.25-inch, 2HD</td><td>μS5A10AS17K</td></tr>
<tr><td>3.5-inch, 2HD</td><td>μS5A13AS17K</td></tr>
<tr><td rowspan="2">IBM PC/AT</td><td colspan="2" rowspan="2">PC DOS™</td><td>5.25-inch, 2HC</td><td>μS7B10AS17K</td></tr>
<tr><td>3.5-inch, 2HC</td><td>μS7B13AS17K</td></tr>
<tr><td rowspan="4">Device file (AS17133)</td><td rowspan="4">AS17133 is a device file for the μPD17133 and μPD17P133 .
It is used together with the assembler (AS17K), which is applicable to the 17K series.</td><td rowspan="2">PC-9800 series</td><td colspan="2" rowspan="2">MS-DOS</td><td>5.25-inch, 2HD</td><td>μS5A10AS17120 Note</td></tr>
<tr><td>3.5-inch, 2HD</td><td>μS5A13AS17120 Note</td></tr>
<tr><td rowspan="2">IBM PC/AT</td><td colspan="2" rowspan="2">PC DOS</td><td>5.25-inch, 2HC</td><td>μS7B10AS17120 Note</td></tr>
<tr><td>3.5-inch, 2HC</td><td>μS7B13AS17120 Note</td></tr>
<tr><td rowspan="4">Support software (SIMPLEHOST)</td><td rowspan="4">SIMPLEHOST, running on the Windows™, provides man-machine-interface in developing programs by using a personal computer and the in-circuit emulator.</td><td rowspan="2">PC-9800 series</td><td rowspan="2">MS-DOS</td><td rowspan="4">Windows</td><td>5.25-inch, 2HD</td><td>μS5A10IE17K</td></tr>
<tr><td>3.5-inch, 2HD</td><td>μS5A13IE17K</td></tr>
<tr><td rowspan="2">IBM PC/AT</td><td rowspan="2">PC DOS</td><td>5.25-inch, 2HC</td><td>μS7B10IE17K</td></tr>
<tr><td>3.5-inch, 2HC</td><td>μS7B13IE17K</td></tr>
</table>

Note μS××××AS17120 indicates the AS17120, AS17121, AS17132, and AS17133.

★ **Remark** The following table lists the versions of the operating systems described in the above table.

OS	Versions
MS-DOS	Ver. 3.30 to Ver. 5.00A Note
PC DOS	Ver. 3.1 to Ver. 5.0 Note
Windows	Ver. 3.0 to Ver. 3.1

Note MS-DOS versions 5.00 and 5.00A and PC DOS Ver. 5.0 are provided with a task swap function. This function, however, cannot be used in these software packages.

Cautions on CMOS Devices

Countermeasures against static electricity for all MOSs

Caution When handling MOS devices, take care so that they are not electrostatically charged.
Strong static electricity may cause dielectric breakdown in gates. When transporting or storing MOS devices, use conductive trays, magazine cases, shock absorbers, or metal cases that NEC uses for packaging and shipping. Be sure to ground MOS devices during assembling. Do not allow MOS devices to stand on plastic plates or do not touch pins. Also handle boards on which MOS devices are mounted in the same way.

$ **CMOS-specific handling of unused input pins**

Caution Hold CMOS devices at a fixed input level.
Unlike bipolar or NMOS devices, if a CMOS device is operated with no input, an intermediate-level input may be caused by noise. This allows current to flow in the CMOS device, resulting in a malfunction. Use a pull-up or pull-down resistor to hold a fixed input level. Since unused pins may function as output pins at unexpected times, each unused pin should be separately connected to the V_{DD} or GND pin through a resistor.
If handling of unused pins is documented, follow the instructions in the document.

% **Statuses of all MOS devices at initialization**

Caution The initial status of a MOS device is unpredictable when power is turned on.
Since characteristics of a MOS device are determined by the amount of ions implanted in molecules, the initial status cannot be determined in the manufacture process. NEC has no responsibility for the output statuses of pins, input and output settings, and the contents of registers at power on. However, NEC assures operation after reset and items for mode setting if they are defined.
When you turn on a device having a reset function, be sure to reset the device first.