NEC

MOS INTEGRATED CIRCUIT

μPD78F0058,78F0058Y

8-BIT SINGLE-CHIP MICROCONTROLLERS

DESCRIPTION

The μPD78F0058 is a product of the μPD780058 Subseries in the 78K/0 Series and equivalent to the μPD780058 with a flash memory in place of internal ROM. This device is incorporated with a flash memory which can be programmed without being removed from the substrate.

The μPD78F0058Y is a products based on the μPD78F0058, with an I^2C bus interface supporting multimaster.

Functions are described in detail in the following user's manuals, which should be read when carrying out design work.

μPD780058, 780058Y Subseries User's Manual	**:U12013E**
78K/0 Series User's Manual Instruction	**:U12326E**

FEATURES

- Pin-compatible with mask ROM version (except V_{PP} pin)
- Flash memory : 60 Kbytes[Note 1]
- Internal high-speed RAM : 1024 bytes
- Internal expansion RAM : 1024 bytes[Note 2]
- Buffer RAM : 32 bytes
- Power supply voltage : V_{DD} = 2.7 to 5.5 V

Notes 1. The flash memory capacity can be changed with the memory size switching register (IMS).

2. The internal expansion RAM capacity can be changed with the internal expansion RAM size switching register (IXS).

Remark For the differences between the flash memory versions and the mask ROM versions, refer to **1. DIFFERENCES BETWEEN μPD78F0058, 78F0058Y, AND MASK ROM VERSION.**

APPLICATION FIELDS

Car audio systems, cellular phones, pagers, printers, AV equipment, cameras, PPCs, vending machines, etc.

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The mark ★ shows major revised points.

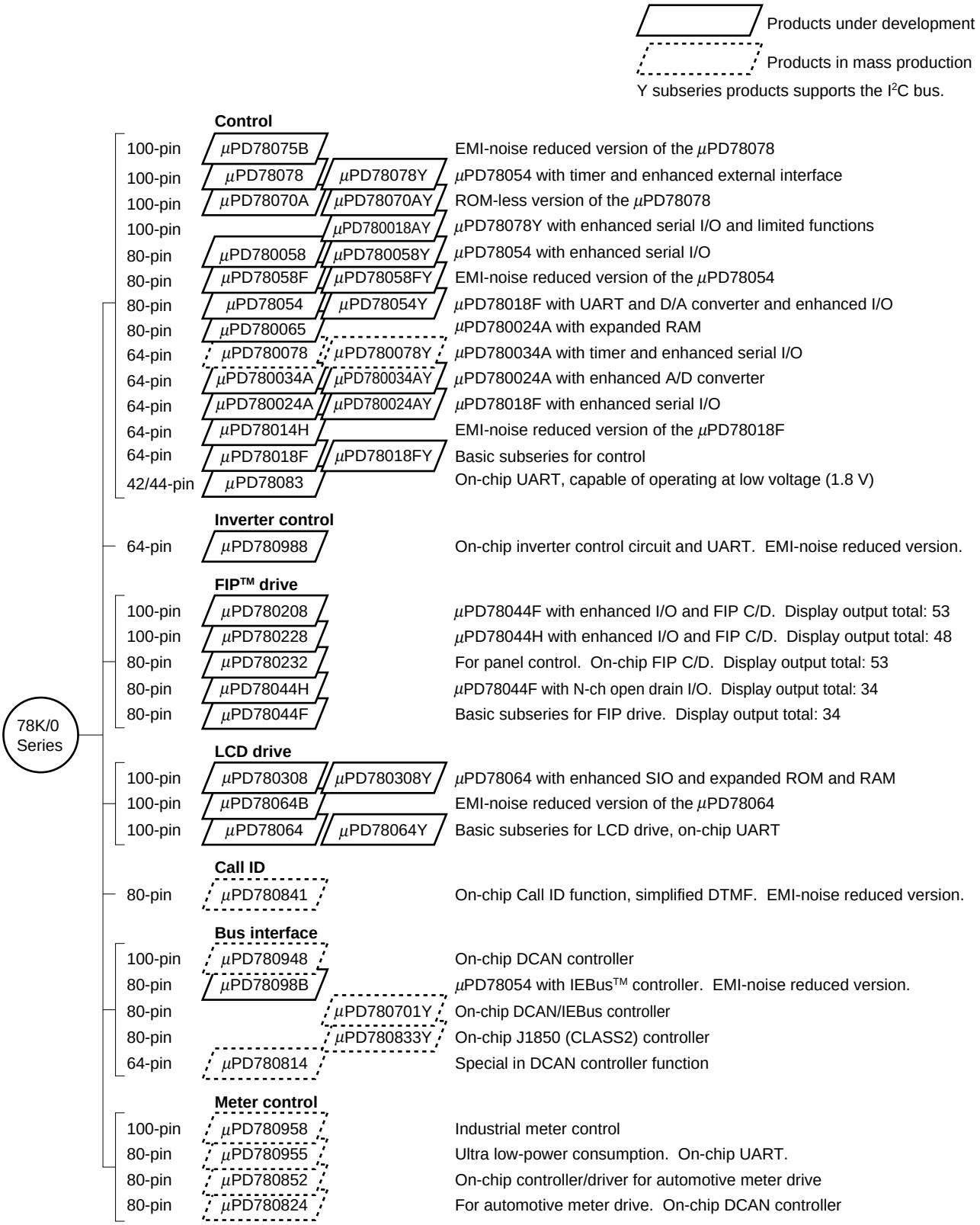
ORDERING INFORMATION

	Part Number	Package
	μPD78F0058GC-8BT	80-pin plastic QFP (14 × 14 mm)
	μPD78F0058GK-BE9	80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness 1.05 mm)
★	μPD78F0058GK-9EU[Note]	80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness 1.0 mm)
	μPD78F0058YGC-8BT	80-pin plastic QFP (14 × 14 mm)
	μPD78F0058YGK-BE9	80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness 1.05 mm)
★	μPD78F0058YGK-9EU[Note]	80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness 1.0 mm)

Note Under development

★ 78K/0 SERIES LINEUP

The products in the 78K/0 Series are listed below. The names enclosed in boxes are subseries name.



The major functional differences among the subseries are listed below.

Subseries Name \ Function		ROM Capacity	Timer				8-Bit A/D	10-Bit A/D	8-Bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
			8-bit	16-bit	Watch	WDT							
Control	μPD78075B	32 K to 40K	4 ch	1 ch	1 ch	1 ch	8 ch	–	2 ch	3 ch (UART: 1 ch)	88	1.8 V	√
	μPD78078	48 K to 60K											
	μPD78070A	–									61	2.7 V	
	μPD780058	24 K to 60 K	2 ch							3 ch (time-division UART: 1 ch)	68	1.8 V	
	μPD78058F	48 K to 60 K								3 ch (UART: 1 ch)	69	2.7 V	
	μPD78054	16 K to 60 K										2.0 V	
	μPD780065	40 K to 48 K							–	4 ch (UART: 1 ch)	60	2.7 V	
	μPD780078	48 K to 60 K		2 ch			–	8 ch		3 ch (UART: 2 ch)	52	1.8 V	
	μPD780034A	8 K to 32 K		1 ch						3 ch (UART: 1 ch)	51		
	μPD780024A						8 ch	–					
	μPD78014H									2 ch	53		
	μPD78018F	8 K to 60 K											
	μPD78083	8 K to 16 K		–	–					1 ch (UART: 1 ch)	33		–
Inverter control	μPD780988	16 K to 60 K	3 ch	**Note**	–	1 ch	–	8 ch	–	3 ch (UART: 2 ch)	47	4.0 V	√
FIP drive	μPD780208	32 K to 60 K	2 ch	1 ch	1 ch	1 ch	8 ch	–	–	2 ch	74	2.7 V	–
	μPD780228	48 K to 60 K	3 ch	–	–					1 ch	72	4.5 V	
	μPD780232	16 K to 24 K					4 ch			2 ch	40		
	μPD78044H	32 K to 48 K	2 ch	1 ch	1ch		8 ch			1 ch	68	2.7 V	
	μPD78044F	16 K to 40 K								2 ch			
LCD drive	μPD780308	48 K to 60 K	2 ch	1 ch	1ch	1 ch	8 ch	–	–	3 ch (time-division UART: 1 ch)	57	2.0 V	–
	μPD78064B	32 K								2 ch (UART: 1 ch)			
	μPD78064	16 K to 32 K											
Call ID	μPD780841	24 K to 32 K	1 ch	1 ch	1 ch	1 ch	2 ch	–	–	2 ch (UART: 1 ch)	57	2.7 V	–
Bus interface supported	μPD780948	60 K	2 ch	2 ch	1 ch	1 ch	8 ch	–	–	3 ch (UART: 1 ch)	79	4.0 V	√
	μPD78098B	40 K to 60 K		1 ch					2 ch		69	2.7 V	–
	μPD780814	32 K to 60 K		2 ch			12 ch		–	2 ch (UART: 1 ch)	46	4.0 V	
Meter control	μPD780958	48 K to 60 K	4 ch	2 ch	–	1 ch	–	–	–	2 ch (UART: 1 ch)	69	2.2 V	–
	μPD780955	40 K	6 ch	1 ch			1 ch			2 ch (UART: 2 ch)	50		
	μPD780852	32 K to 40 K	3 ch		1 ch		5 ch			3 ch (UART: 1 ch)	56	4.0 V	
	μPD780824	32 K to 60 K								2 ch (UART: 1 ch)	59	4.0 V	

Note 16-bit timer: 2 channels
10-bit timer: 1 channel

The major functional differences among the Y subseries are shown below.

Subseries Name \ Function		ROM Capacity	Configuration of Serial Interface	I/O	V_{DD} MIN. Value
Control	μPD78078Y	48 K to 60 K	3-wire/2-wire/I²C : 1 ch 3-wire with automatic transmit/receive function : 1 ch 3-wire/UART : 1 ch	88	1.8 V
	μPD78070AY	–		61	2.7 V
	μPD780018AY	48 K to 60 K	3-wire with automatic transmit/receive function : 1 ch Time-division 3-wire : 1 ch I²C bus (multimaster supported) : 1 ch	88	
	μPD780058Y	24 K to 60 K	3-wire/2-wire/I²C : 1 ch 3-wire with automatic transmit/receive function : 1 ch 3-wire/time-division UART : 1 ch	68	1.8 V
	μPD78058FY	48 K to 60 K	3-wire/2-wire/I²C : 1 ch 3-wire with automatic transmit/receive function : 1 ch 3-wire/UART : 1 ch	69	2.7 V
	μPD78054Y	16 K to 60 K			2.0 V
	μPD780078Y	48 K to 60 K	3-wire : 1 ch UART : 1 ch 3-wire/UART : 1 ch I²C bus (multimaster supported) : 1 ch	52	1.8 V
	μPD780034AY	8 K to 32 K	UART : 1 ch 3-wire : 1 ch I²C bus (multimaster supported) : 1 ch	51	1.8 V
	μPD780024AY				
	μPD78018FY	8 K to 60 K	3-wire/2-wire/I²C : 1 ch 3-wire with automatic transmit/receive function : 1 ch	53	
LCD drive	μPD780308Y	48 K to 60 K	3-wire/2-wire/I²C : 1 ch 3-wire/time-division UART : 1 ch 3-wire : 1 ch	57	2.0 V
	μPD78064Y	16 K to 32 K	3-wire/2-wire/I²C : 1 ch 3-wire/UART : 1 ch		

Remark The functions other than the serial interface are common to the Subseries without Y.

OVERVIEW OF FUNCTIONS

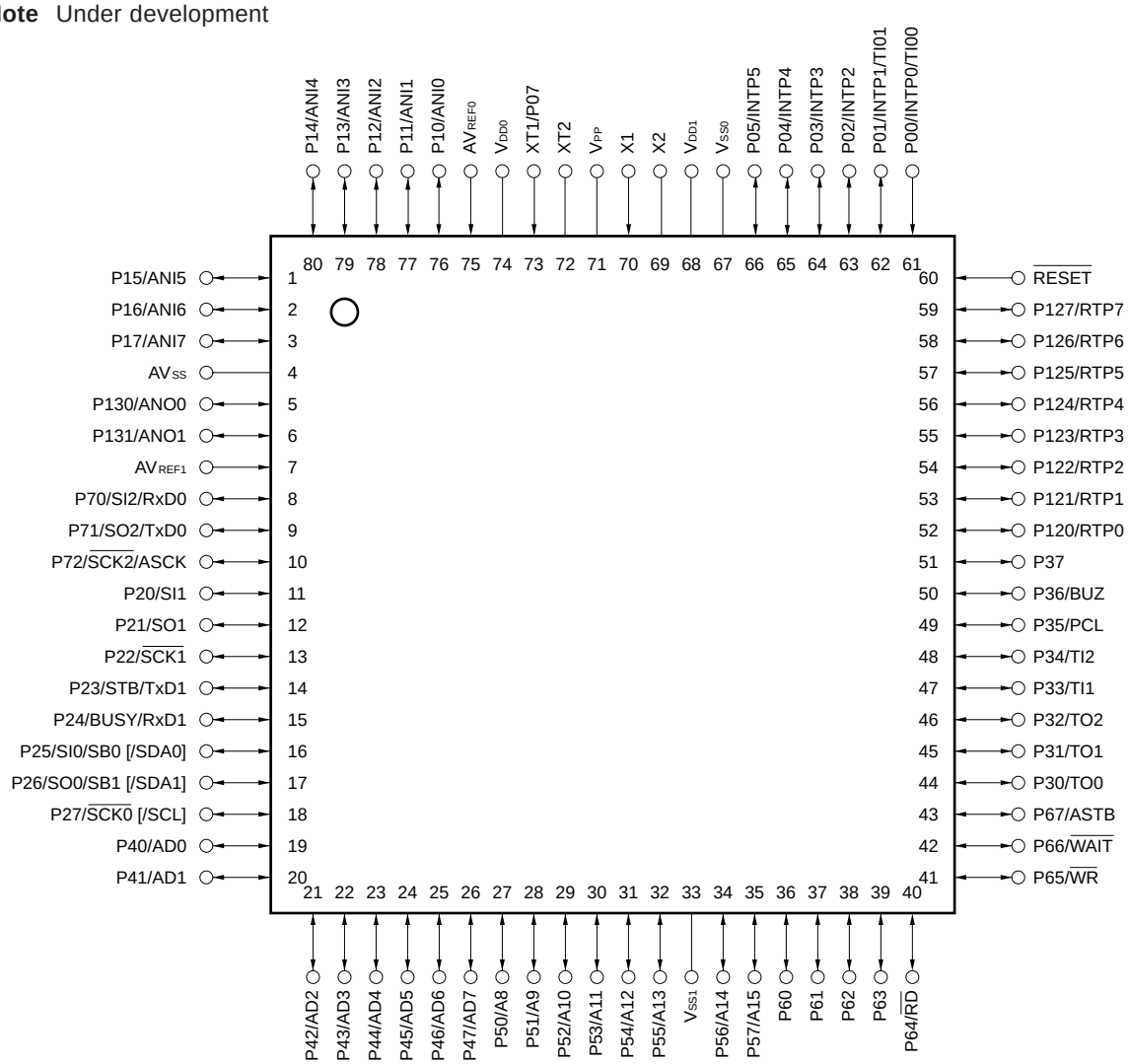
Item \ Product Name		μPD78F0058	μPD78F0058Y
Internal memory	Flash memory	60 Kbytes	
	High-speed RAM	1,024 bytes	
	Buffer RAM	32 bytes	
	Expanded RAM	1,024 bytes	
Memory space		64 Kbytes	
General registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)	
Minimum instruction execution time	When main system clock is selected	0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (@5.0 MHz operation)	
	When subsystem clock is selected	122 μs (@32.768 kHz operation)	
Instruction set		• 16-bit operation • Multiply/divide (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, Boolean operation) • BCD adjust, etc.	
I/O ports		Total: 68 • CMOS input: 2 • CMOS I/O: 62 • N-ch open-drain I/O: 4	
★ A/D converter		• 8-bit resolution × 8 channels (V_{DD} = 2.7 to 5.5 V)	
★ D/A converter		• 8-bit resolution × 2 channels (V_{DD} = 2.7 to 5.5 V)	
★ Serial interface		• 3-wire serial I/O/SBI/2-wire serial I/O mode selectable: 1 channel	• 3-wire serial I/O/2-wire serial I/O/I^2C mode selectable: 1 channel
		• 3-wire serial I/O mode (automatic data transmit/receive function for up to 32 bytes provided on chip): 1 channel • 3-wire/serial I/O/UART mode (time division transfer function provided on chip) selectable: 1 channel	
Timers		• 16-bit timer/event counter: 1 channel • 8-bit timer/event counter: 2 channels • Watch timer: 1 channel • Watchdog timer: 1 channel	
Timer outputs		3 (14-bit PWM output × 1)	
Clock output		19.5 kHz, 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz, 2.5 MHz, 5.0 MHz (@5.0 MHz operation with main system clock) 32.768 kHz (@32.768 kHz operation with subsystem clock)	
Buzzer output		1.2 kHz, 2.4 kHz, 4.9 kHz, 9.8 kHz (@5.0 MHz operation with main system clock)	
★ Vectored interrupt sources	Maskable	Internal: 13, External: 6	
	Non-maskable	Internal: 1	
	Software	1	
Test inputs		Internal: 1, External: 1	
Supply voltage		V_{DD} = 2.7 to 5.5 V	
Operating ambient temperature		T_A = –40 to +85°C	
Package		• 80-pin plastic QFP (14 × 14 mm) • 80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness 1.05 mm) ★ • 80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness 1.0 mm)	

CONTENTS

1. PIN CONFIGURATION (TOP VIEW)

- **80-pin plastic QFP (14 × 14 mm)**
  μPD78F0058GC-8BT, 78F0058YGC-8BT
- **80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness 1.05 mm)**
  μPD78F0058GK-BE9, 78F0058YGK-BE9
- ★ **80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness 1.0 mm)**
  μPD78F0058GK-9EU**Note**, 78F0058YGK-9EU**Note**

Note Under development



Cautions 1. Connect the V_{PP} pin directly to V_{SS0} or V_{SS1} in normal operation mode.

2. Connect the AV_{SS} pin to V_{SS0}.

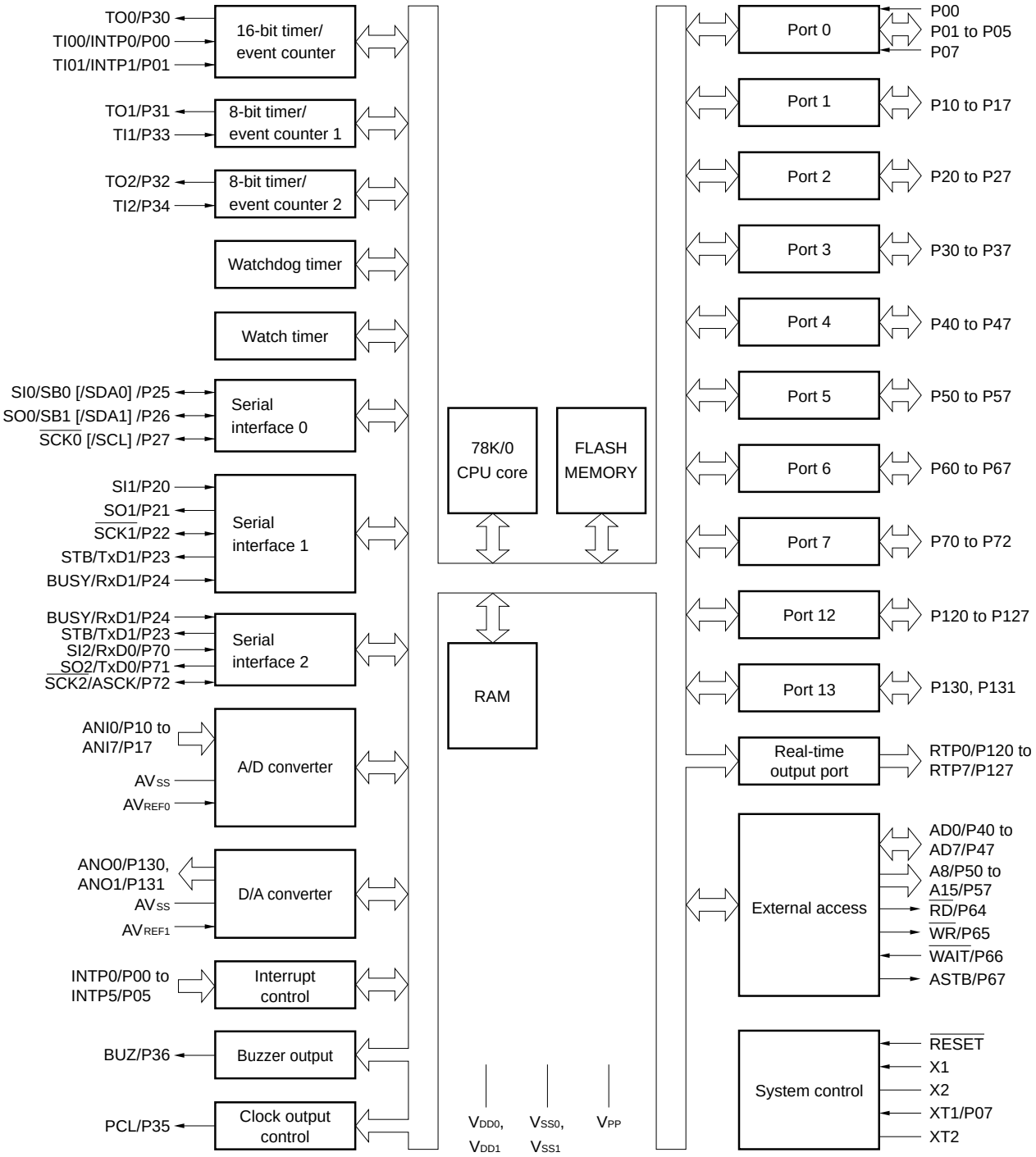
Remarks 1. [ ]: μPD78F0058Y only.

2. When the microcontroller is used in applications where the noise generated inside the microcontroller needs to be reduced, the implementation of noise reduction measures, such as supplying voltage to V_{DD0} and V_{DD1} individually and connecting V_{SS0} and V_{SS1} to different ground lines, is recommended.

PIN IDENTIFICATION

A8 to A15	: Address Bus	$\overline{RD}$	: Read Strobe
AD0 to AD7	: Address/Data Bus	$\overline{RESET}$	: Reset
ANI0 to ANI7	: Analog Input	RTP0 to RTP7	: Real-Time Output Port
ANO0, ANO1	: Analog Output	RxD0, RxD1	: Receive Data
ASCK	: Asychronous Serial Clock	SB0, SB1	: Serial Bus
ASTB	: Address Strobe	$\overline{SCK0}$ to $\overline{SCK2}$	: Serial Clock
AV_{REF0}, AV_{REF1}	: Analog Reference Voltage	SCL	: Serial Clock
AV_{SS}	: Analog Ground	SDA0, SDA1	: Serial Data
BUSY	: Busy	SI0 to SI2	: Serial Input
BUZ	: Buzzer Clock	SO0 to SO2	: Serial Output
INTP0 to INTP5	: Interrupt from Peripherals	STB	: Strobe
P00 to P05, P07	: Port 0	TI00, TI01	: Timer Input
P10 to P17	: Port 1	TI1, TI2	: Timer Input
P20 to P27	: Port 2	TO0 to TO2	: Timer Output
P30 to P37	: Port 3	TxD0, TxD1	: Transmit Data
P40 to P47	: Port 4	V_{DD0}, V_{DD1}	: Power Supply
P50 to P57	: Port 5	V_{PP}	: Programming Power Supply
P60 to P67	: Port 6	V_{SS0}, V_{SS1}	: Ground
P70 to P72	: Port 7	$\overline{WAIT}$	: Wait
P120 to P127	: Port 12	$\overline{WR}$	: Write Strobe
P130, P131	: Port 13	X1, X2	: Crystal (Main System Clock)
PCL	: Programmable Clock	XT1, XT2	: Crystal (Subsystem Clock)

2. BLOCK DIAGRAM



Remark [ ]: μPD78F0058Y only.

3. DIFFERENCES BETWEEN μPD78F0058, 78F0058Y, AND MASK ROM VERSIONS

The μPD78F0058 and 78F0058Y are products provided with a flash memory which enables on-board reading, erasing, and rewriting of programs with device mounted on target system. The functions of the μPD78F0058 and 78F0058Y (except the functions specified for flash memory and mask option of P60 to P63 pins) can be made the same as those of the mask ROM versions by setting the memory size switching register (IMS) and internal expansion RAM size switching register (IXS).

Table 3-1 shows the differences between the flash memory version (μPD78F0058, 78F0058Y) and the mask ROM versions (μPD780053, 780054, 780055, 780056, 780058, 780053Y, 780054Y, 780055Y,780056Y, and 780058Y).

Table 3-1. Differences between μPD78F0058, 78F0058Y and Mask ROM Versions

	Item	μPD78F0058	μPD78F0058Y	Mask ROM Versions	
				μPD780058 Subseries	μPD780058Y Subseries
	Internal ROM structure	Flash memory		Mask ROM	
	Internal ROM capacity	60 Kbytes		μPD780053, 780053Y : 24 Kbytes μPD780054, 780054Y : 32 Kbytes μPD780055, 780055Y : 40 Kbytes μPD780056, 780056Y : 48 Kbytes μPD780058, 780058Y : 60 Kbytes	
	Internal expansion RAM capacity	1024 bytes		μPD780053, 780053Y : None μPD780054, 780054Y : None μPD780055, 780055Y : None μPD780056, 780056Y : None μPD780058, 780058Y : 1024 bytes	
	Internal ROM capacity changeable/not changeable with memory size switching register (IMS)	Changeable[Note 1]		Not changeable	
	Internal expansion RAM capacity changeable/not changeable with internal expansion RAM size switching register (IXS)	Changeable[Note 2]		Not changeable	
★	Supply voltage	V_{DD} = 2.7 to 5.5 V		V_{DD} = 1.8 to 5.5 V	
	IC pin	Not provided		Provided	
	V_{PP} pin	Provided		Not provided	
	P60 to P63 pin mask option with internal pull-up resistors	Not provided		Provided	
★	Serial interface (SBI)	Provided	Not provided	Provided	Not provided
★	Serial interface (I^2C)	Not provided	Provided	Not provided	Provided

Notes 1. Flash memory is set to 60 Kbytes by $\overline{\text{RESET}}$ input.

2. Internal expansion RAM is set to 1024 bytes by $\overline{\text{RESET}}$ input.

Caution The noise resistance and noise radiation differ between flash memory versions and mask ROM versions. When considering the replacement of flash memory versions with mask ROM versions in the process from trial manufacturing to mass production, adequate evaluation should be carried out using CS products (not ES products) of mask ROM versions.

Remark Only the μPD780058, 780058Y, 78F0058, and 78F0058Y are provided with IXS.

3.1 Memory Size Switching Register (IMS)

This register sets a part of internal memory unused by software. The memory mapping can be made the same as that of mask ROM versions with different types of internal memory (ROM and RAM) by setting the memory size switching register (IMS).

The IMS is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets the IMS to CFH.

Figure 3-1. Format of Memory Size Switching Register

Symbol	7	6	5	4	3	2	1	0	Address	At reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	CFH	R/W

ROM3	ROM2	ROM1	ROM0	Selection of Internal ROM Capacity
0	1	1	0	24 Kbytes
1	0	0	0	32 Kbytes
1	0	1	0	40 Kbytes
1	1	0	0	48 Kbytes
1	1	1	0	56 Kbytes[Note]
1	1	1	1	60 Kbytes
Others				Setting prohibited

RAM2	RAM1	RAM0	Selection of Internal High-speed RAM Capacity
1	1	0	1024 bytes
Others			Setting prohibited

Note When using external device expansion function, set the internal ROM capacity to less than 56 Kbytes.

Table 3-2 shows the IMS set value to make the memory mapping the same as those of mask ROM versions.

Table 3-2. Set Value of Memory Size Switching Register

Target Mask ROM Versions	IMS Set Value
μPD780053, 780053Y	C6H
μPD780054, 780054Y	C8H
μPD780055, 780055Y	CAH
μPD780056, 780056Y	CCH
μPD780058, 780058Y	CFH

3.2 Internal Expansion RAM Size Switching Register (IXS)

This register sets the internal expansion RAM capacity by software. The memory mapping can be made the same as that of mask ROM versions with different types of internal expansion RAM by setting the internal expansion RAM size switching register (IXS).

The IXS is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets the IXS to 0AH.

Figure 3-2. Format of Internal Expansion RAM Size Switching Register

Symbol	7	6	5	4	3	2	1	0	Address	At reset	R/W
IXS	0	0	0	0	IXRAM3	IXRAM2	IXRAM1	IXRAM0	FFF4H	0AH	W

IXRAM3	IXRAM2	IXRAM1	IXRAM0	Selection of Internal Expansion RAM Capacity
1	1	0	0	0 bytes
1	0	1	0	1024 bytes
Others				Setting prohibited

Table 3-3 shows the IXS set value to make the memory mapping the same as those of mask ROM versions.

Table 3-3. Set Value of Internal Expansion RAM Size Switching Register

Target Mask ROM Versions	IMS Set Value
μPD780053, 780053Y	0CH
μPD780054, 780054Y	
μPD780055, 780055Y	
μPD780056, 780056Y	
μPD780058, 780058Y	0AH

4. PIN FUNCTIONS

4.1 Port Pins (1/2)

Pin Name	I/O	Function		After Reset	Alternate Function
P00	Input	Port 0 7-bit input/output port	Input only	Input	INTP0/TI00
P01	I/O		Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.	Input	INTP1/TI01
P02					INTP2
P03					INTP3
P04					INTP4
P05					INTP5
P07[Note 1]	Input		Input only	Input	XT1
P10 to P17	I/O	Port 1 8-bit input/output port Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software[Note 2].		Input	ANI0 to ANI7
P20	I/O	Port 2 8-bit input/output port Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.		Input	SI1
P21					SO1
P22					$\overline{\text{SCK1}}$
P23					STB/TxD1
P24					BUSY/RxD1
P25					SI0/SB0 [/SDA0]
P26					SO0/SB1 [/SDA1]
P27					$\overline{\text{SCK0}}$ [/SCL]
P30	I/O	Port 3 8-bit input/output port Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.		Input	TO0
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					–
P40 to P47	I/O	Port 4 8-bit input/output port Input/output can be specified in 8-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software. The test input flag (KRIF) is set to 1 by falling edge detection.		Input	AD0 to AD7

Notes 1. When using the P07/XT1 pins as an input port, set bit 6 (FRC) of the processor clock control register (PCC) to 1. Do not use the on-chip feedback resistor of the subsystem clock oscillator.

2. When using the P10/ANI0 to P17/ANI7 pins as the A/D converter analog input pins, set port 1 to the input mode. At this time, on-chip pull-up resistors are automatically disconnected.

Remark [ ]: μPD78F0058Y only.

4.1 Port Pins (2/2)

Pin Name	I/O	Function		After Reset	Alternate Function
P50 to P57	I/O	Port 5 8-bit input/output port LEDs can be driven directly. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.		Input	A8 to A15
P60	I/O	Port 6 8-bit input/outport port Input/output can be specified in 1-bit units.	N-ch open-drain input/output port LEDs can be driven directly.	Input	–
P61					
P62					
P63					
P64			When used as an input port, an on-chip pull-up resistor can be specified by means of software.		$\overline{RD}$
P65					$\overline{WR}$
P66					$\overline{WAIT}$
P67					ASTB
P70	I/O	Port 7 3-bit input/output port Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.		Input	SI2/RxD0
P71					SO2/TxD0
P72					$\overline{SCK2}$/ASCK
P120 to P127	I/O	Port 12 8-bit input/output port Input/output can be specified in 1-bit units. When used as an input port, on-chip pull-up resistor can be specified by means of software.		Input	RTP0 to RTP7
P130, P131	I/O	Port 13 2-bit input/output port Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.		Input	ANO0, ANO1

4.2 Non-Port Pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising edge and falling edges) can be specified.	Input	P00/TI00
INTP1				P01/TI01
INTP2				P02
INTP3				P03
INTP4				P04
INTP5				P05
SI0	Input	Serial interface serial data input	Input	P25/SB0 [/SDA0]
SI1				P20
SI2				P70/RxD
SO0	Output	Serial interface serial data output	Input	P26/SB1 [/SDA1]
SO1				P21
SO2				P71/TxD
SB0	I/O	Serial interface serial data input/output	Input	P25/SI0 [/SDA0]
SB1				P26/SO0 [/SDA1]
★ SDA0		μPD78F0058Y only		P25/SI0/SB0
★ SDA1				P26/SO0/SB1
$\overline{SCK0}$	I/O	Serial interface serial clock input/output	Input	P27 [/SCL]
$\overline{SCK1}$				P22
$\overline{SCK2}$				P72/ASCK
★ SCL		μPD78F0058Y only		P27/$\overline{SCK0}$
STB	Output	Serial interface automatic transmit/receive strobe output	Input	P23/TxD1
BUSY	Input	Serial interface automatic transmit/receive busy input	Input	P24/RxD1
RxD0	Input	Asynchronous serial interface serial data input	Input	P70/SI2
RxD1				P24/BUSY
TxD0	Output	Asynchronous serial interface serial data output	Input	P71/SO2
TxD1				P23/STB
ASCK	Input	Asynchronous serial interface serial clock input	Input	P72/$\overline{SCK2}$
TI00	Input	External count clock input to the 16-bit timer (TM0)	Input	P00/INTP0
TI01		Capture trigger signal input to the capture register (CR00)		P01/INTP1
TI1		External count clock input to the 8-bit timer (TM1)		P33
TI2		External count clock input to the 8-bit timer (TM2)		P34
TO0	Output	16-bit timer (TM0) output (also used for 14-bit PWM output)	Input	P30
TO1		8-bit timer (TM1) output		P31
TO2		8-bit timer (TM2) output		P32
PCL	Output	Clock output (for trimming of main system clock and subsystem clock)	Input	P35
BUZ	Output	Buzzer output	Input	P36
RTP0 to RTP7	Output	Real-time output port from which data is output in synchronization with a trigger	Input	P120 to P127
AD0 to AD7	I/O	Lower address/data bus for expanding memory externally	Input	P40 to P47

Remark [ ]: μPD78F0058Y only.

4.2 Non-Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
A8 to A15	Output	Higher address bus for expanding memory externally	Input	P50 to P57
$\overline{RD}$	Output	Strobe signal output for reading from external memory	Input	P64
$\overline{WR}$		Strobe signal output for writing to external memory		P65
$\overline{WAIT}$	Input	Wait insertion at external memory access	Input	P66
ASTB	Output	Strobe output that externally latches address information output to ports 4 and 5 to access external memory.	Input	P67
ANI0 to ANI7	Input	A/D converter analog input	Input	P10 to P17
ANO0, ANO1	Output	D/A converter analog output	Input	P130, P131
AV_{REF0}	Input	A/D converter reference voltage input (also used for analog power supply)	–	–
AV_{REF1}	Input	D/A converter reference voltage input	–	–
AV_{SS}	–	A/D converter and D/A converter ground potential Use at the same potential as V_{SS0}.	–	–
$\overline{RESET}$	Input	System reset input	–	–
X1	Input	Connecting crystal resonator for main system clock oscillation	–	–
X2	–		–	–
XT1	Input	Connecting crystal resonator for subsystem clock oscillation	Input	P07
XT2	–		–	–
V_{DD0}	–	Port block positive power supply	–	–
V_{SS0}	–	Port block ground potential	–	–
V_{DD1}	–	Positive power supply (except for port and analog blocks)	–	–
V_{SS1}	–	Ground potential (except for port and analog blocks)	–	–
V_{PP}	–	Setting flash memory programming mode. Applying high voltage for program write/verify. Connect directly to V_{SS0} or V_{SS1} in normal operation mode.	–	–

4.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 4-1. For the input/output circuit configuration of each type, see Figure 4-1.

Table 4-1. Input/Output Circuit Type of Each Pin (1/2)

Pin Name	Input/Output Circuit Type	I/O	Recommended Connection
P00/INTP0/TI00	2	Input	Connect to V_{SS0}.
P01/INTP1/TI01	8-C	I/O	Input : Independently connect to V_{SS0} via a resistor. Output : Leave open.
P02/INTP2			
P03/INTP3			
P04/INTP4			
P05/INTP5			
P07/XT1	16	Input	Connect to V_{DD0}.
P10/ANI0 to P17/ANI7	11-D	I/O	Input : Independently connect to V_{DD0} or V_{SS0} via a resistor. Output : Leave open.
P20/SI1	8-C		
P21/SO1	5-H		
P22/$\overline{SCK1}$	8-C		
P23/STB/TxD1	5-H		
P24/BUSY/RxD1	8-C		
P25/SI0/SB0 [/SDA0]	10-B		
P26/SO0/SB1 [/SDA1]			
P27/$\overline{SCK0}$ [/SCL]			
P30/TO0	5-H		
P31/TO1			
P32/TO2			
P33/TI1	8-C		
P34/TI2			
P35/PCL	5-H		
P36/BUZ			
P37			
P40/AD0 to P47/AD7	5-N		Input : Independently connect to V_{DD0} via a resistor. Output : Leave open.
P50/A8 to P57/A15	5-H		Input : Independently connect to V_{DD0} or V_{SS0} via a resistor. Output : Leave open.
P60 to P63	13-K		Input : Independently connect to V_{DD0} via a resistor. Output : Leave open.
P64/$\overline{RD}$	5-H		Input : Independently connect to V_{DD0} or V_{SS0} via a resistor. Output : Leave open.
P65/$\overline{WR}$			
P66/$\overline{WAIT}$			
P67/ASTB			

Remark [ ]: μPD78F0058Y only.

Table 4-1. Input/Output Circuit Type of Each Pin (2/2)

Pin Name	Input/Output Circuit Type	I/O	Recommended Connection
P70/SI2/RxD0	8-C	I/O	Input : Independently connect to V_{DD0} or V_{SS0} via a resistor. Output : Leave open.
P71/SO2/TxD0	5-H		
P72/$\overline{SCK2}$/ASCK	8-C		
P120/RTP0 to P127/RTP7	5-H		
P130/ANO0, P131/ANO1	12-C		Input : Independently connect to V_{SS0} via a resistor. Output : Leave open.
$\overline{RESET}$	2	Input	–
XT2	16	–	Leave open.
AV_{REF0}	–		Connect to V_{SS0}.
AV_{REF1}			Connect to V_{DD0}.
AV_{SS}			Connect to V_{SS0}.
V_{PP}			Connect directly to V_{SS0} or V_{SS1}.

Figure 4-1. Pin Input/Output Circuits (1/2)

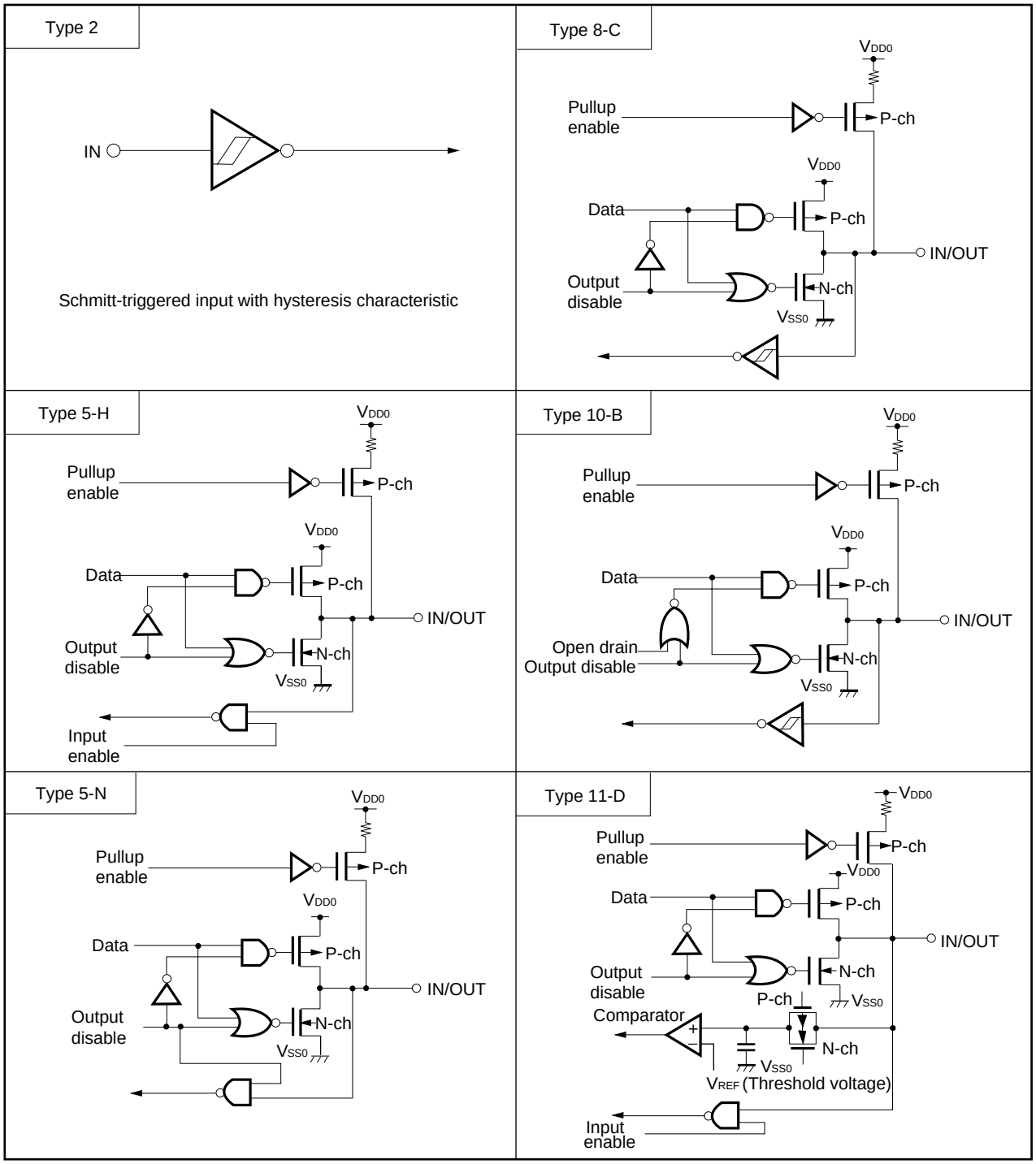
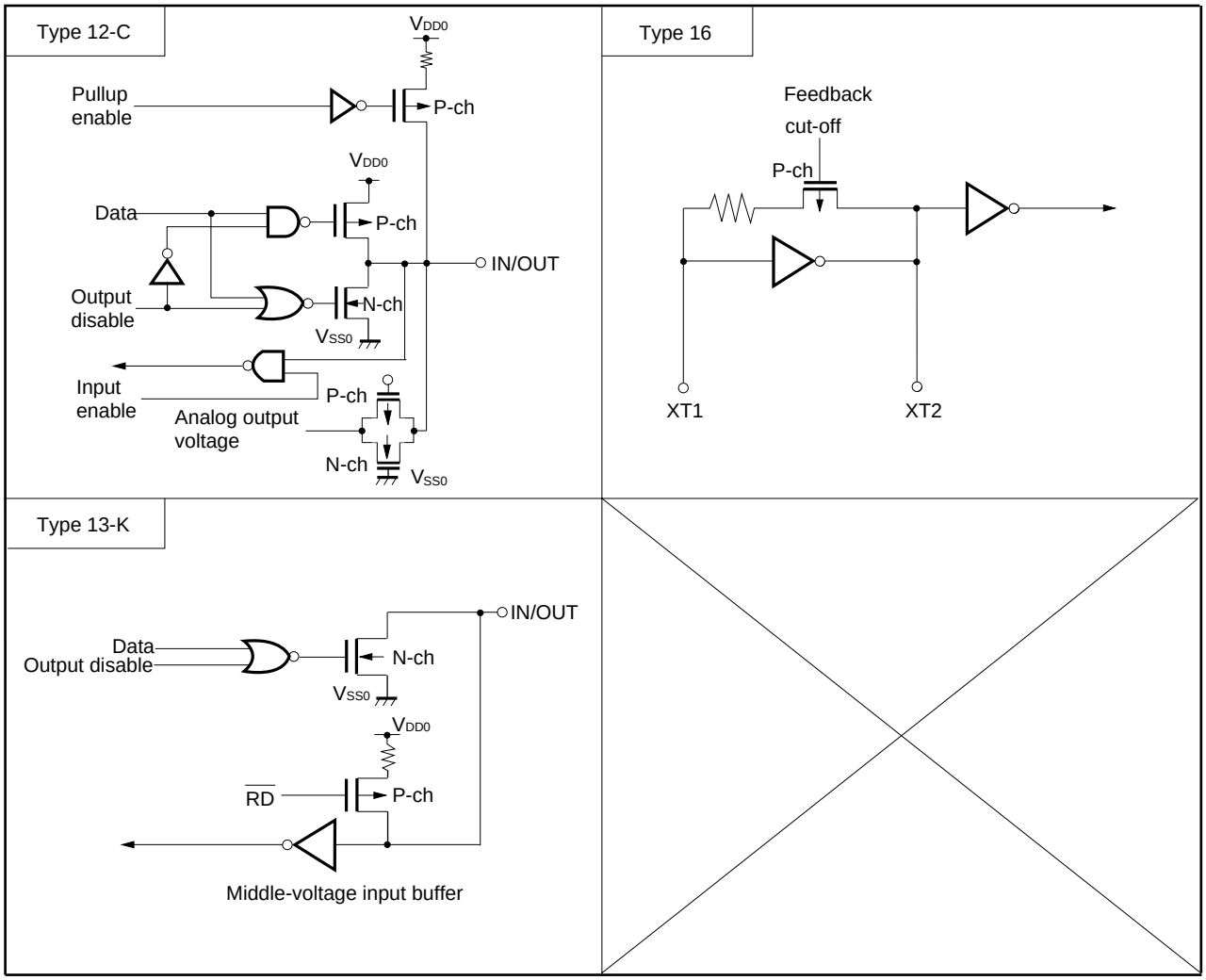


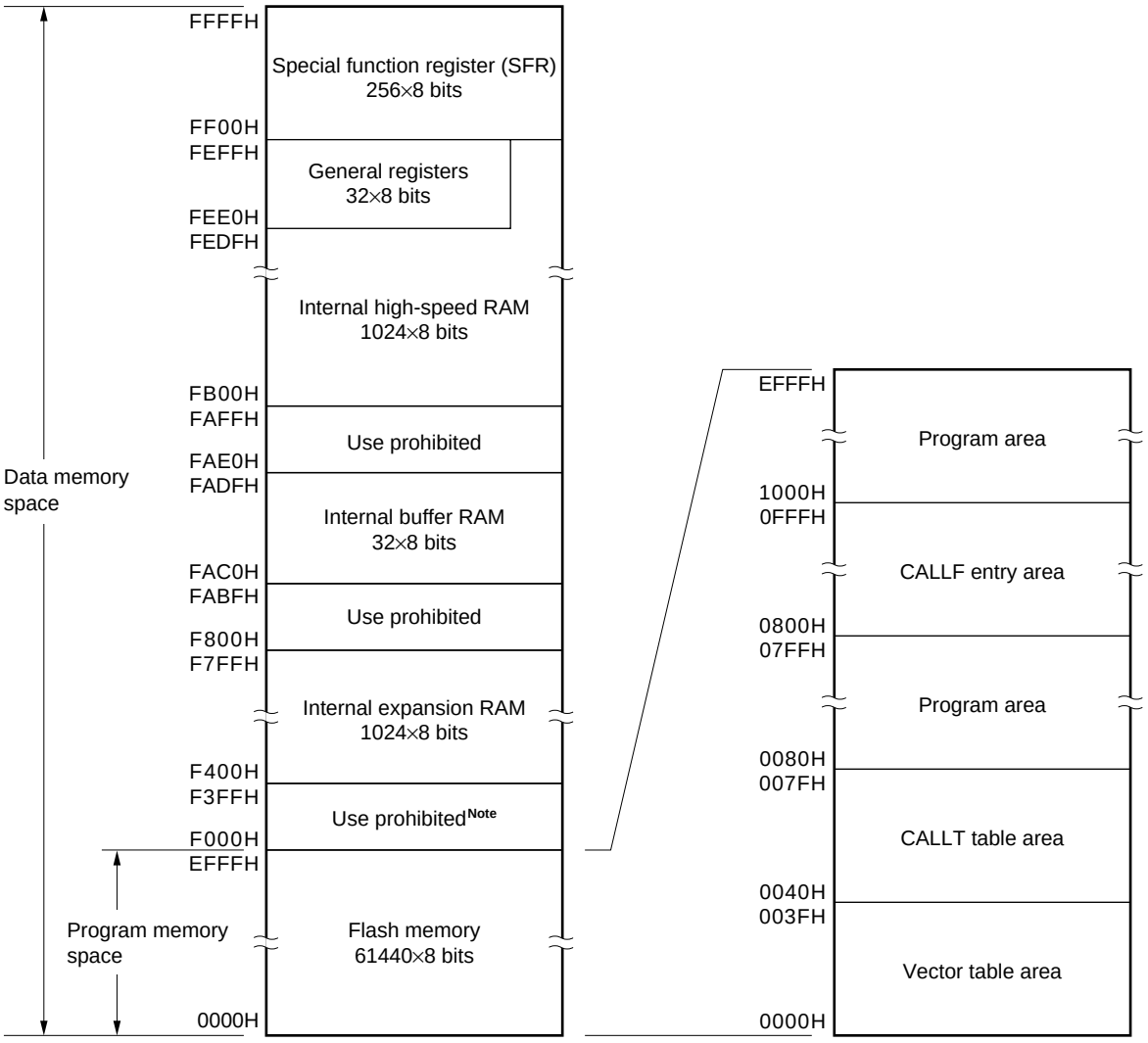
Figure 4-1. Pin Input/Output Circuits (2/2)



★ 5. MEMORY SPACE

Figure 5-1 shows the memory map of the μPD78F0058 and 78F0058Y.

Figure 5-1. Memory Map



Note The area between F000H and F3FFH cannot be used when the flash memory size is 60 Kbytes. This area can be used by setting the flash memory size to 56 Kbytes or less with the memory size switching register (IMS).

6. FLASH MEMORY PROGRAMMING

The program memory provided in the μPD78F0058 and 78F0058Y is flash memory.

Writing to a flash memory can be performed without removing the memory from the target system (on-board).

★ Writing is performed connecting the dedicated flash programmer (Flashpro III (part number : FL-PR3, PG-FP3) to the host machine and the target system.

Remark FL-PR3 is a product of Naito Densei Machida Mfg. Co., Ltd.

6.1 Selection of Transmission Mode

Writing to a flash memory is performed using the Flashpro III with a serial transmission mode. One of the transmission mode is selected from those in Table 6-1. The selection of the transmission mode is made by using the format shown in Figure 6-1. Each transmission mode is selected by the number of V_{PP} pulses shown in Table 6-1.

Table 6-1. List of Transmission Mode

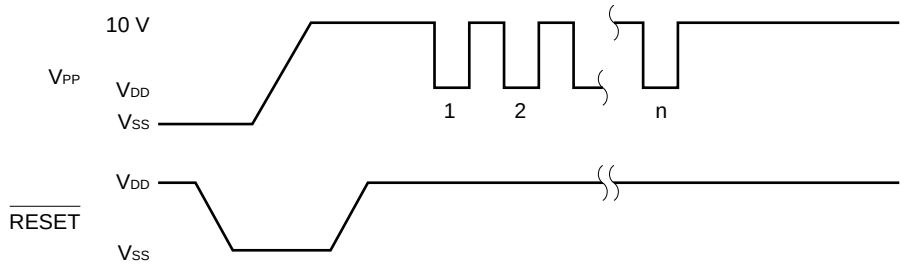
Transmission Mode	Channels	Pin	V_{PP} Pulses
3-wire serial I/O	3	P27/$\overline{SCK0}$ [/SCL]	0
		P26/SO0/SB1 [/SDA1]	
		P25/SI0/SB0 [/SDA0]	
		P22/$\overline{SCK1}$	1
		P21/SO1	
		P20/SI1	
		P72/$\overline{SCK2}$/ASCK	2
		P71/SO2/TxD0	
		P70/SI1/RxD0	
UART	2	P71/SO2/TxD0	8
		P70/SI2/RxD0	
		P23/TxD1	9
		P24/RxD1	
Pseudo 3-wire serial I/O[Note]	1	P32/TO2 (serial clock input/output)	12
		P31/TO1 (serial data output)	
		P30/TO0 (serial data input)	

Note Serial transmission is performed by controlling the port using software.

Caution Select a communication mode always using the number of V_{PP} pulses shown in Table 6-1.

Remark [ ] : μPD78F0058Y only.

Figure 6-1. Format of Transmission Mode Selection



★ 6.2 Function of Flash Memory Programming

Operations such as writing to a flash memory are performed by various command/data transmission and reception operations according to the selected transmission mode. Table 6-2 shows major functions of flash memory programming.

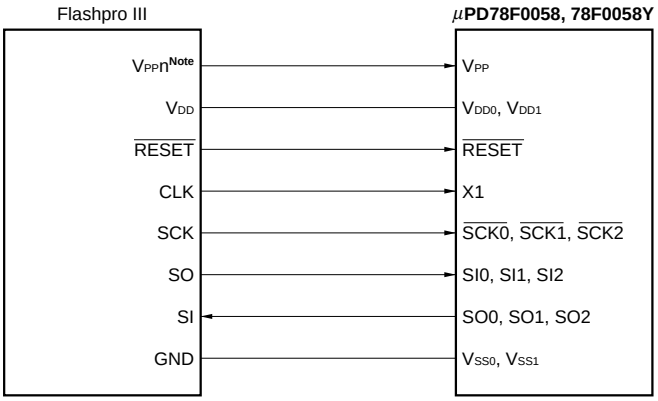
Table 6-2. Major Functions of Flash Memory Programming

Functions	Descriptions
Batch delete	Deletes the entire memory contents.
Batch blank check	Checks the deletion status of the entire memory.
Data write	Performs write to the flash memory based on the write start address and the number of data to be written (number of bytes).
Batch verify	Compares the entire memory contents with the input data.

★ 6.3 Connection of Flashpro III

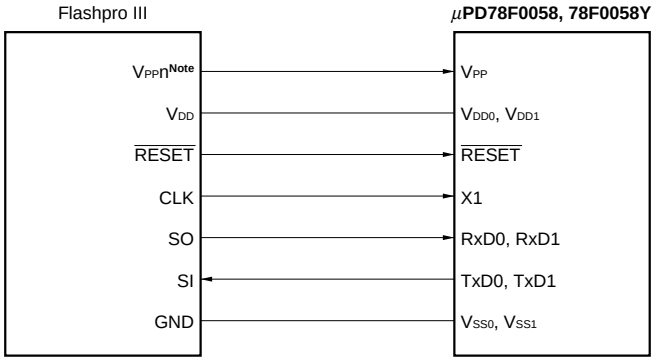
The connection of the Flashpro III and the μPD78F0058 and 78F0058Y differs according to the transmission mode (3-wire serial I/O, UART, pseudo 3-wire). The connection for each transmission mode is shown in Figures 6-2 to 6-4.

Figure 6-2. Connection of Flashpro III for 3-wire Serial I/O Mode



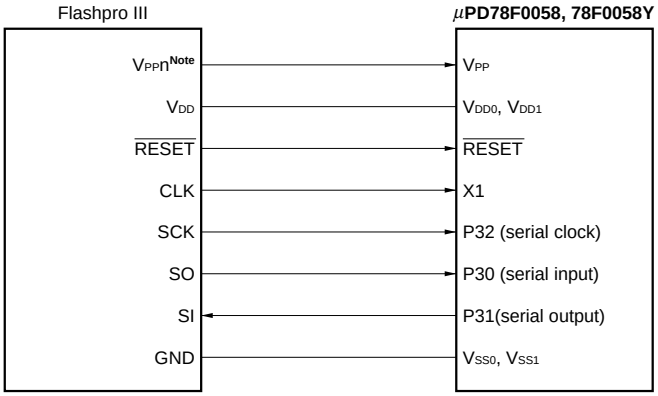
Note n = 1, 2

Figure 6-3. Connection of Flashpro III for UART Mode



Note n = 1, 2

Figure 6-4. Connection of Flashpro III for Pseudo 3-wire Serial I/O Mode



Note n = 1, 2

6.4 Example of Settings for Flashpro III (PG-FP3)

Make the following setting when writing to flash memory using Flashpro III (PG-FP3)

<1> Load the parameter file.
<2> Select serial mode and serial clock using the type command.
<3> An example of the settings for the PG-FP3 is shown below.

Table 6-3. Example of Settings for PG-FP3

Communication Mode	Example of Setting for PG-FP3		Number of V_{PP} Pulses[Note 1]
3-wire serial I/O	COMM PORT	SIO-ch0/1/2	0/1/2
	CPU CLK	On Target Board	
		In Flashpro	
	On Target Board	4.1943 MHz	
	SIO CLK	1.0 MHz	
	In Flashpro	4.0 MHz	
	SIO CLK	1.0 MHz	
UART	COMM PORT	UART-ch0/1	8/9
	CPU CLK	On Target Board	
	On Target Board	4.1943 MHz	
	UART BPS	9600 bps[Note 2]	
Pseudo 3-wire	COMM PORT	PortA	12
	CPU CLK	On Target Board	
		In Flashpro	
	On Target Board	4.1943 MHz	
	SIO CLK	1.0 kHz	
	In Flashpro	4.0 MHz	
	SIO CLK	1.0 kHz	

Notes 1. The number of V_{PP} pulses supplied from Flashpro III when serial communication is initialized. The pins to be used for communication are determined according to the number of these pulses.

2. Select one of 9600 bps, 19200 bps, 38400 bps, or 768000 bps.

Remark COMM PORT : Selection of serial port
SIO CLK : Selection of serial clock frequency
CPU CLK : Selection of source of CPU clock to be input

★ 7. ELECTRICAL SPECIFICATIONS

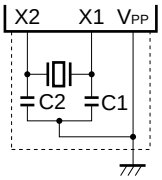
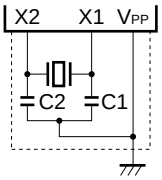
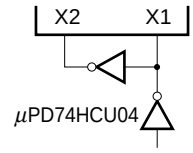
Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}			–0.3 to +6.5	V
	V_{PP}			–0.3 to +10.5	V
	AV_{REF0}			–0.3 to V_{DD} + 0.3	V
	AV_{REF1}			–0.3 to V_{DD} + 0.3	V
	AV_{SS}			–0.3 to +0.3	V
Input voltage	V_{I1}	P00-P05, P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P64-P67, P70-P72, P120-P127, P130, P131, X1, X2, XT2, $\overline{\text{RESET}}$		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P60-P63	N-ch open drain	–0.3 to +16	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	P10-P17	Analog input pin	AV_{SS} – 0.3 to AV_{REF0} + 0.3	V
Output current, high	I_{OH}	Per pin		–10	mA
		Total for P01-P05, P30-P37, P56, P57, P60-P67, P120-P127		–15	mA
		Total for P10-P17, P20-P27, P40-P47, P50-P55, P70-P72, P130, P131		–15	mA
Output current, low	I_{OL}**Note**	Per pin	Peak value	30	mA
			rms value	15	mA
		Total for P50-P55	Peak value	100	mA
			rms value	70	mA
		Total for P56, P57, P60-P63	Peak value	100	mA
			rms value	70	mA
		Total for P10-P17, P20-P27, P40-P47, P70-P72, P130, P131	Peak value	50	mA
			rms value	20	mA
		Total for P01-P05, P30-P37, P64-P67, P120-P127	Peak value	50	mA
			rms value	20	mA
Operating ambient temperature	T_A	During normal operation		–40 to +85	°C
		During flash memory programming		10 to 40	°C
Storage temperature	T_{stg}			–65 to +125	°C

Note The rms value should be calculated as follows: [rms value] = [Peak value] × $\sqrt{\text{Duty}}$

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Main System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)**Note 1**	V_{DD} = Oscillation voltage range	1.0		5.0	MHz
		Oscillation stabilization time**Note 2**	After V_{DD} reaches oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequency (f_X)**Note 1**		1.0		5.0	MHz
		Oscillation stabilization time**Note 2**	V_{DD} = 4.5 to 5.5 V			10	ms
						30	
External clock		X1 input frequency (f_X)**Note 1**		1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})		85		500	ns

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release.

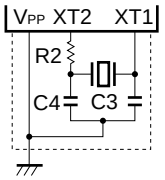
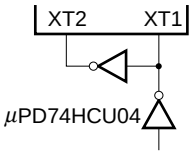
Cautions 1. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS1}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main system clock is stopped and the system is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Subsystem Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})Note 1		32	32.768	35	kHz
		Oscillation stabilization time Note 2	V_{DD} = 4.5 to 5.5 V		1.2	2	s
						10	
External clock		XT1 input frequency (f_{XT})Note 1		32		100	kHz
		XT1 input high-/low-level width (t_{XTH}, t_{XTL})		5		15	μs

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after V_{DD} reaches oscillation voltage range MIN.

Cautions 1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS1}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subsystem clock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V.				15	pF
I/O capacitance	C_{IO}	f = 1 MHz Unmeasured pins returned to 0 V.	P01-P05, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P64-P67, P70-P72, P120-P127, P130, P131			15	pF
			P60-P63			20	pF

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P10-P17, P21, P23, P30-P32, P35-P37, P40-P47, P50-P57, P64-P67, P71, P120-P127, P130, P131	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		V_{DD}	V
	V_{IH2}	P00-P05, P20, P22, P24-P27, P33, P34, P70, P72, $\overline{\text{RESET}}$	V_{DD} = 2.7 to 5.5 V	0.8V_{DD}		V_{DD}	V
	V_{IH3}	P60-P63 (N-ch open drain)	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		15	V
	V_{IH4}	X1, X2	V_{DD} = 2.7 to 5.5 V	V_{DD} – 0.5		V_{DD}	V
	V_{IH5}	XT1/P07, XT2	4.5 V ≤ V_{DD} ≤ 5.5 V	0.8V_{DD}		V_{DD}	V
			2.7 V ≤ V_{DD} < 4.5 V	0.9V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P10-P17, P21, P23, P30-P32, P35-P37, P40-P47, P50-P57, P64-P67, P71, P120-P127, P130, P131	V_{DD} = 2.7 to 5.5 V	0		0.3V_{DD}	V
	V_{IL2}	P00-P05, P20, P22, P24-P27, P33, P34, P70, P72, $\overline{\text{RESET}}$	V_{DD} = 2.7 to 5.5 V	0		0.2V_{DD}	V
	V_{IL3}	P60-P63	4.5 V ≤ V_{DD} ≤ 5.5 V	0		0.3V_{DD}	V
			2.7 V ≤ V_{DD} < 4.5 V	0		0.2V_{DD}	V
	V_{IL4}	X1, X2	V_{DD} = 2.7 to 5.5 V	0		0.4	V
	V_{IL5}	XT1/P07, XT2	4.5 V ≤ V_{DD} ≤ 5.5 V	0		0.2V_{DD}	V
			2.7 V ≤ V_{DD} < 4.5 V	0		0.1V_{DD}	V
Output voltage, high	V_{OH}	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1 mA		V_{DD} – 1.0			V
		I_{OH} = –100 μA		V_{DD} – 0.5			V
Output voltage, low	V_{OL1}	P50-P57, P60-P63	V_{DD} = 4.5 to 5.5 V, I_{OL} = 15 mA		0.4	2.0	V
		P01-P05, P10-P17, P20-P27, P30-P37, P40-P47, P64-P67, P70-P72, P120-P127, P130, P131	V_{DD} = 4.5 to 5.5 V, I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	SB0, SB1, $\overline{\text{SCK0}}$	V_{DD} = 4.5 to 5.5 V, open drain, pulled-up (R = 1 kΩ)			0.2V_{DD}	V
	V_{OL3}	I_{OL} = 400 μA				0.5	V

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	$V_{IN} = V_{DD}$	P00-P05, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P72, P120-P127, P130, P131, $\overline{\text{RESET}}$			3	μA
	I_{LIH2}		X1, X2, XT1/P07, XT2			20	μA
	I_{LIH3}	V_{IN} = 15 V	P60 to P63			80	μA
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	P00-P05, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P64-P67, P70-P72, P120-P127, P130, P131, $\overline{\text{RESET}}$			–3	μA
	I_{LIL2}		X1, X2, XT1/P07, XT2			–20	μA
	I_{LIL3}		P60-P63			–3 Note 1	μA
Output leakage current, high	I_{LOH}	$V_{OUT} = V_{DD}$				3	μA
Output leakage current, low	I_{LOL}	V_{OUT} = 0 V				–3	μA
Software pull-up resistor Note 2	R	V_{IN} = 0 V, P01-P05, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P64-P67, P70-P72, P120-P127, P130, P131		15	30	90	kΩ

Notes 1. A low-level input leakage current of –200 μA (MAX.) flows only for 1.5 clocks (without wait) after a read instruction has been executed to port 6 (P6) or port mode register 6 (PM6). At times other than this 1.5-clock interval, a –3 μA (MAX.) current flows.

2. Software pull-up resistor can only be used within the range V_{DD} = 2.7 to 5.5 V.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Power supply current[Note 5]	I_{DD1}[Note 5]	5.0 MHz crystal oscillation operating mode (f_{XX} = 2.5 MHz)[Note 3]	V_{DD} = 5.0 V ±10%[Note 1]		6.2	12.5	mA
			V_{DD} = 3.0 V ±10%[Note 2]		1.3	3.1	mA
		5.0 MHz crystal oscillation operating mode (f_{XX} = 5.0 MHz)[Note 4]	V_{DD} = 5.0 V ±10%[Note 1]		13.1	25.7	mA
			V_{DD} = 3.0 V ±10%[Note 2]		2.1	4.9	mA
	I_{DD2}	5.0 MHz crystal oscillation HALT mode (f_{XX} = 2.5 MHz)[Note 3]	V_{DD} = 5.0 V ±10%				
			Peripheral functions operating			5.6	mA
			Peripheral functions not operating		1.0	2.8	mA
			V_{DD} = 3.0 V ±10%				
			Peripheral functions operating			2.9	mA
			Peripheral functions not operating		0.44	1.1	mA
		5.0 MHz crystal oscillation HALT mode (f_{XX} = 5.0 MHz)[Note 4]	V_{DD} = 5.0 V ±10%				
			Peripheral functions operating			8.4	mA
			Peripheral functions not operating		1.3	3.1	mA
			V_{DD} = 3.0 V ±10%				
			Peripheral functions operating			4.5	mA
			Peripheral functions not operating		0.6	1.5	mA
	I_{DD3}[Note 5]	32.768 kHz crystal oscillation operating mode[Note 6]	V_{DD} = 5.0 V ±10%		110	220	μA
			V_{DD} = 3.0 V ±10%		86	172	μA
	I_{DD4}[Note 5]	32.768 kHz crystal oscillation HALT mode[Note 6]	V_{DD} = 5.0 V ±10%		22.5	45	μA
			V_{DD} = 3.0 V ±10%		3.2	6.4	μA
	I_{DD5}[Note 5]	XT1 = V_{DD} STOP mode When feedback resistor is used	V_{DD} = 5.0 V ±10%		1.0	30	μA
			V_{DD} = 3.0 V ±10%		0.5	10	μA
	I_{DD6}[Note 5]	XT1 = V_{DD} STOP mode When feedback resistor is not used	V_{DD} = 5.0 V ±10%		0.1	30	μA
			V_{DD} = 3.0 V ±10%		0.05	10	μA

Notes 1. High-speed mode operation (when the processor clock control register (PCC) is set to 00H).

2. Low-speed mode operation (when PCC is set to 04H).

3. Operation with main system clock $f_{XX} = f_X/2$ (when the oscillation mode select register (OSMS) is set to 00H)

4. Operation with main system clock $f_{XX} = f_X$ (when OSMS is set to 01H)

5. Refers to the current flowing to the V_{DD0} and V_{DD1} pins. The current flowing to the A/D converter, D/A converter, and on-chip pull-up resistor is not included.

6. When the main system clock operation is stopped.

AC Characteristics

(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (Min. instruction execution time)	T_{CY}	Operating with main system clock (f_{XX} = 2.5 MHz)Note 1	V_{DD} = 2.7 to 5.5 V	0.8		64	μs
		Operating with main system clock (f_{XX} = 5.0 MHz)Note 2	3.5 V ≤ V_{DD} ≤ 5.5 V	0.4		32	μs
			2.7 V ≤ V_{DD} < 3.5 V	0.8		32	μs
		Operating with subsystem clock		40Note 3	122	125	μs
TI00 input high-/low-level width	t_{TIH00}	3.5 V ≤ V_{DD} ≤ 5.5 V		$2/f_{sam}$ + 0.1Note 4			μs
	t_{TIL00}	2.7 V ≤ V_{DD} < 3.5 V		$2/f_{sam}$ + 0.2Note 4			μs
TI01 input high-/low-level width	t_{TIH01} t_{TIL01}	V_{DD} = 2.7 to 5.5 V		10			μs
TI1, TI2 input frequency	f_{TI1}	V_{DD} = 4.5 to 5.5 V		0		4	MHz
				0		275	kHz
TI1, TI2 input high-/low-level width	t_{TIH1}	V_{DD} = 4.5 to 5.5 V		100			ns
	t_{TIL1}			1.8			μs
Interrupt request input high-/low-level width	t_{INTH} t_{INTL}	INTP0	3.5 V ≤ V_{DD} ≤ 5.5 V	$2/f_{sam}$ + 0.1Note 4			μs
			2.7 V ≤ V_{DD} < 3.5 V	$2/f_{sam}$ + 0.2Note 4			μs
		INTP1-INTP5, P40-P47	V_{DD} = 2.7 to 5.5 V	10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}	V_{DD} = 2.7 to 5.5 V		10			μs

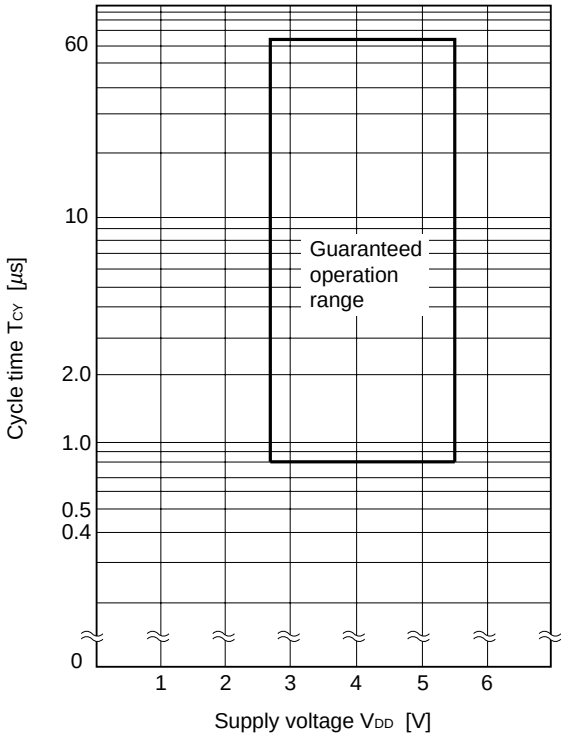
Notes 1. Operation with main system clock $f_{XX} = f_X/2$ (when the oscillation mode select register (OSMS) is set to 00H)

2. Operation with main system clock $f_{XX} = f_X$ (when OSMS is set to 01H)

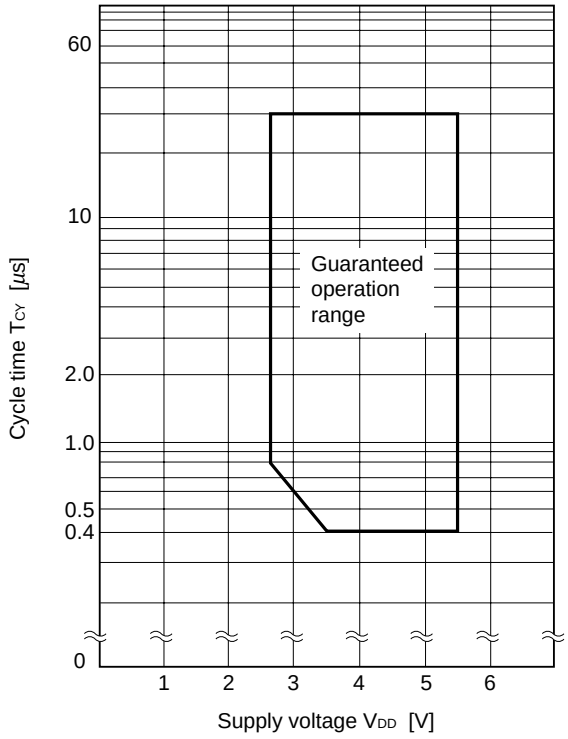
3. Value when external clock is used. When a crystal resonator is used, it is 114 μs (MIN.)

4. Selection of $f_{sam} = f_{XX}/2^N$, $f_{XX}/32$, $f_{XX}/64$, and $f_{XX}/128$ is possible with bits 0 and 1 (SCS0, SCS1) of the sampling clock select register (SCS) (when N= 0 to 4).

T_{CY} vs. V_{DD} (@f_{XX} = f_X/2 main system clock operation)



T_{CY} vs. V_{DD} (@f_{XX} = f_X main system clock operation)



(2) Read/write operation

(a) When MCS = 1, PCC2 to PCC0 = 000B (T_A = –40 to +85°C, V_{DD} = 3.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.85t_{CY}$ – 50		ns
Address setup time	t_{ADS}		$0.85t_{CY}$ – 50		ns
Address hold time	t_{ADH}		50		ns
Data input time from address	t_{ADD1}			$(2.85 + 2n)t_{CY}$ – 80	ns
	t_{ADD2}			$(4 + 2n)t_{CY}$ – 100	ns
Data input time from $\overline{RD}$↓	t_{RDD1}			$(2 + 2n)t_{CY}$ – 100	ns
	t_{RDD2}			$(2.85 + 2n)t_{CY}$ – 100	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		$(2 + 2n)t_{CY}$ – 60		ns
	t_{RDL2}		$(2.85 + 2n)t_{CY}$ – 60		ns
$\overline{WAIT}$↓ input time from $\overline{RD}$↓	t_{RDWT1}			$0.85t_{CY}$ – 50	ns
	t_{RDWT2}			$2t_{CY}$ – 60	ns
$\overline{WAIT}$↓ input time from $\overline{WR}$↓	t_{WRWT}			$2t_{CY}$ – 60	ns
$\overline{WAIT}$ low-level width	t_{WTL}		$(1.15 + 2n)t_{CY}$	$(2 + 2n)t_{CY}$	ns
Write data setup time	t_{WDS}		$(2.85 + 2n)t_{CY}$ – 100		ns
Write data hold time	t_{WDH}		20		ns
$\overline{WR}$ low-level width	t_{WRL}		$(2.85 + 2n)t_{CY}$ – 60		ns
$\overline{RD}$↓ delay time from ASTB↓	t_{ASTRD}		25		ns
$\overline{WR}$↓ delay time from ASTB↓	t_{ASTWR}		$0.85t_{CY}$ + 20		ns
ASTB↑ delay time from $\overline{RD}$↑ at external fetch	t_{RDAST}		$0.85t_{CY}$ – 10	$1.15t_{CY}$ + 20	ns
Address hold time from $\overline{RD}$↑ at external fetch	t_{RDADH}		$0.85t_{CY}$ – 50	$1.15t_{CY}$ + 50	ns
Write data output time from $\overline{RD}$↑	t_{RDWD}		40		ns
Write data output time from $\overline{WR}$↓	t_{WRWD}		0	50	ns
Address hold time from $\overline{WR}$↑	t_{WRADH}		$0.85t_{CY}$	$1.15t_{CY}$ + 40	ns
$\overline{RD}$↑ delay time from $\overline{WAIT}$↑	t_{WTRD}		$1.15t_{CY}$ + 40	$3.15t_{CY}$ + 40	ns
$\overline{WR}$↑ delay time from $\overline{WAIT}$↑	t_{WTWR}		$1.15t_{CY}$ + 30	$3.15t_{CY}$ + 30	ns

Remarks 1. MCS: Bit 0 of the oscillation mode select register (OSMS)

2. PCC2 to PCC0: Bits 2 to 0 of the processor clock control register (PCC)

3. $t_{CY} = T_{CY}/4$

4. n indicates the number of waits.

(b) When MCS = 0 or PCC2 to PCC0 ≠ 000B (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		t_{CY} – 80		ns
Address setup time	t_{ADS}		t_{CY} – 80		ns
Address hold time	t_{ADH}		0.4t_{CY} – 10		ns
Data input time from address	t_{ADD1}			(3 + 2n)t_{CY} – 160	ns
	t_{ADD2}			(4 + 2n)t_{CY} – 200	ns
Data input time from $\overline{RD}\downarrow$	t_{RDD1}			(1.4 + 2n)t_{CY} – 70	ns
	t_{RDD2}			(2.4 + 2n)t_{CY} – 70	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		(1.4 + 2n)t_{CY} – 20		ns
	t_{RDL2}		(2.4 + 2n)t_{CY} – 20		ns
$\overline{WAIT}\downarrow$ input time from $\overline{RD}\downarrow$	t_{RDWT1}			t_{CY} – 100	ns
	t_{RDWT2}			2t_{CY} – 100	ns
$\overline{WAIT}\downarrow$ input time from $\overline{WR}\downarrow$	t_{WRWT}			2t_{CY} – 100	ns
$\overline{WAIT}$ low-level width	t_{WTL}		(1 + 2n)t_{CY}	(2 + 2n)t_{CY}	ns
Write data setup time	t_{WDS}		(2.4 + 2n)t_{CY} – 60		ns
Write data hold time	t_{WDH}		20		ns
$\overline{WR}$ low-level width	t_{WRL}		(2.4 + 2n)t_{CY} – 20		ns
$\overline{RD}\downarrow$ delay time from ASTB$\downarrow$	t_{ASTRD}		0.4t_{CY} – 30		ns
$\overline{WR}\downarrow$ delay time from ASTB$\downarrow$	t_{ASTWR}		1.4t_{CY} – 30		ns
ASTB$\uparrow$ delay time from $\overline{RD}\uparrow$ at external fetch	t_{RDAST}		t_{CY} – 10	t_{CY} + 20	ns
Address hold time from $\overline{RD}\uparrow$ at external fetch	t_{RDADH}		t_{CY} – 50	t_{CY} + 50	ns
Write data output time from $\overline{RD}\uparrow$	t_{RDWD}		0.4t_{CY} – 20		ns
Write data output time from $\overline{WR}\downarrow$	t_{WRWD}		0	60	ns
Address hold time from $\overline{WR}\uparrow$	t_{WRADH}		t_{CY}	t_{CY} + 60	ns
$\overline{RD}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTRD}		0.6t_{CY} + 180	2.6t_{CY} + 180	ns
$\overline{WR}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTWR}		0.6t_{CY} + 120	2.6t_{CY} + 120	ns

Remarks 1. MCS: Bit 0 of the oscillation mode select register (OSMS)

2. PCC2 to PCC0: Bits 2 to 0 of the processor clock control register (PCC)

3. $t_{CY} = T_{CY}/4$

4. n indicates the number of waits.

(3) Serial interface (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

(a) Serial interface channel 0

(i) 3-wire serial I/O mode ($\overline{SCK0}$... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY1}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1,600			ns
$\overline{SCK0}$ high-/low-level width	t_{KH1}, t_{KL1}	V_{DD} = 4.5 to 5.5 V	t_{KCY1}/2 – 50			ns
			t_{KCY1}/2 – 100			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK1}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI1}		400			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO1}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of the $\overline{SCK0}$ and SO0 output lines.

(ii) 3-wire serial I/O mode ($\overline{SCK0}$... External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY2}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1,600			ns
$\overline{SCK0}$ high-/low-level width	t_{KH2}, t_{KL2}	4.5 V ≤ V_{DD} ≤ 5.5 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK2}	2.7 V ≤ V_{DD} ≤ 5.5 V	100			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI2}		400			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO2}	C = 100 pF[Note]			300	ns
$\overline{SCK0}$ rise/fall time	t_{R2}, t_{F2}	When using external device expansion function			160	ns
		When not using external device expansion function			1,000	ns

Note C is the load capacitance of the SO0 output line.

(iii) 2-wire serial I/O mode ($\overline{SCK0}$... Internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY3}	R = 1 kΩ, C = 100 pF[Note]	2.7 V ≤ V_{DD} ≤ 5.5 V	1,600			ns
$\overline{SCK0}$ high-level width	t_{KH3}		V_{DD} = 2.7 to 5.5 V	t_{KCY3}/2 – 160			ns
$\overline{SCK0}$ low-level width	t_{KL3}		V_{DD} = 4.5 to 5.5 V	t_{KCY3}/2 – 50			ns
				t_{KCY3}/2 – 100			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK3}		4.5 V ≤ V_{DD} ≤ 5.5 V	300			ns
			2.7 V ≤ V_{DD} < 4.5 V	350			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI3}			600			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO3}			0		300	ns

Note R and C are the load resistance and load capacitance of the $\overline{SCK0}$, SB0, and SB1 output lines.

(iv) 2-wire serial I/O mode ($\overline{SCK0}$... External clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY4}	2.7 V ≤ V_{DD} ≤ 5.5 V		1,600			ns
$\overline{SCK0}$ high-level width	t_{KH4}	2.7 V ≤ V_{DD} ≤ 5.5 V		650			ns
$\overline{SCK0}$ low-level width	t_{KL4}	2.7 V ≤ V_{DD} ≤ 5.5 V		800			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK4}	V_{DD} = 2.7 to 5.5 V		100			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI4}			t_{KCY4}/2			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO4}	R = 1 kΩ, C = 100 pF[Note]	4.5 V ≤ V_{DD} ≤ 5.5 V	0		300	ns
			2.7 V ≤ V_{DD} < 4.5 V	0		500	ns
$\overline{SCK0}$ rise/fall time	t_{R4}, t_{F4}	When using external device expansion function				160	ns
		When not using external device expansion function				1,000	ns

Note R and C are the load resistance and load capacitance of the SB0 and SB1 output lines.

(v) SBI mode ($\overline{SCK0}$... Internal clock output) (μPD78F0058 only)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY5}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.7 V ≤ V_{DD} < 4.5 V		3,200			ns
$\overline{SCK0}$ high-/low-level width	t_{KH5}, t_{KL5}	4.5 V ≤ V_{DD} ≤ 5.5 V		t_{KCY5}/2 – 50			ns
		2.7 V ≤ V_{DD} < 4.5 V		t_{KCY5}/2 – 150			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK5}	4.5 V ≤ V_{DD} ≤ 5.5 V		100			ns
		2.7 V ≤ V_{DD} < 4.5 V		300			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI5}			t_{KCY5}/2			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO5}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 4.5 to 5.5 V	0		250	ns
				0		1,000	ns
SB0, SB1↓ from $\overline{SCK0}$↑	t_{KSB}			t_{KCY5}			ns
$\overline{SCK0}$↓ from SB0, SB1↓	t_{SBK}			t_{KCY5}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY5}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY5}			ns

Note R and C are the load resistance and load capacitance of the $\overline{SCK0}$, SB0, and SB1 output lines.

(vi) SBI mode ($\overline{SCK0}$... External clock input) (μPD78F0058 only)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY6}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.7 V ≤ V_{DD} < 4.5 V		3,200			ns
$\overline{SCK0}$ high-/low-level width	t_{KH6}, t_{KL6}	4.5 V ≤ V_{DD} ≤ 5.5 V		400			ns
		2.7 V ≤ V_{DD} < 4.5 V		1,600			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK6}	4.5 V ≤ V_{DD} ≤ 5.5 V		100			ns
		2.7 V ≤ V_{DD} < 4.5 V		300			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI6}			t_{KCY6}/2			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO6}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 4.5 to 5.5 V	0		300	ns
				0		1,000	ns
SB0, SB1↓ from $\overline{SCK0}$↑	t_{KSB}			t_{KCY6}			ns
$\overline{SCK0}$↓ from SB0, SB1↓	t_{SBK}			t_{KCY6}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY6}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY6}			ns
$\overline{SCK0}$ rise/fall time	t_{R6}, t_{F6}	When using external device expansion function				160	ns
		When not using external device expansion function				1,000	ns

Note R and C are the load resistance and load capacitance of the SB0 and SB1 output lines.

(vii) I²C bus mode (SCL... Internal clock output) (μPD78F0058Y only)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCL cycle time	t_{KCY7}	R = 1 kΩ, C = 100 pF[Note]	2.7 V ≤ V_{DD} < 5.5 V	10			μs
SCL high-level width	t_{KH7}		2.7 V ≤ V_{DD} < 5.5 V	t_{KCY7} – 160			μs
SCL low-level width	t_{KL7}		4.5 V ≤ V_{DD} < 5.5 V	t_{KCY7} – 50			ns
			2.7 V ≤ V_{DD} < 4.5 V	t_{KCY7} – 100			ns
SDA0, SDA1 setup time (to SCL↑)	t_{SIK7}		2.7 V ≤ V_{DD} < 5.5 V	200			ns
SDA0, SDA1 hold time (from SCL↓)	t_{KSI7}			0			ns
SDA0, SDA1 output delay time from SCL↓	t_{KSO7}		4.5 V ≤ V_{DD} < 5.5 V	0		300	ns
				0		500	ns
SDA0, SDA1↓ from SCL↑ or SDA0, SDA1↑ from SCL↑	t_{KSB}			200			ns
SCL↓ from SDA0, SDA1↓	t_{SBK}			400			ns
SDA0, SDA1 high-level width	t_{SBH}			500			ns

Note R and C are the load resistance and load capacitance of the SCL, SDA0, and SDA1 output lines.

(viii) I²C bus mode (SCL... External clock input) (μPD78F0058Y only)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCL cycle time	t_{KCY8}			1			μs
SCL high-level width	t_{KH8}			400			ns
SDA0, SDA1 setup time (to SCL↑)	t_{SIK8}			200			ns
SDA0, SDA1 hold time (from SCL↓)	t_{KSI8}			0			ns
SDA0, SDA1 output delay time from SCL↓	t_{KSO8}	R = 1 kΩ, C = 100 pF[Note]	4.5 V ≤ V_{DD} < 5.5 V	0		300	ns
				0		500	ns
SDA0, SDA1↓ from SCL↑ or SDA0, SDA1↑ from SCL↑	t_{KSB}			200			ns
SCL↓ from SDA0, SDA1↓	t_{SBK}			400			ns
SDA0, SDA1 high-level width	t_{SBH}			500			ns

Note R and C are the load resistance and load capacitance of the SDA0 and SDA1 output lines.

(b) Serial interface channel 1

(i) 3-wire serial I/O mode ($\overline{SCK1}$...Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY9}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1,600			ns
$\overline{SCK1}$ high-/low-level width	t_{KH9}, t_{KL9}	V_{DD} = 4.5 to 5.5 V	t_{KCY9}/2 – 50			ns
			t_{KCY9}/2 – 100			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK9}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI9}		400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO9}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of the $\overline{SCK1}$ and SO1 output lines.

(ii) 3-wire serial I/O mode ($\overline{SCK1}$...External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY10}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1,600			ns
$\overline{SCK1}$ high-/low-level width	t_{KH10}, t_{KL10}	4.5 V ≤ V_{DD} ≤ 5.5 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK10}	V_{DD} = 2.7 to 5.5 V	100			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KIS10}		400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO10}	C = 100 pF[Note] V_{DD} = 2.7 to 5.5 V			300	ns
$\overline{SCK1}$ rise/fall time	t_{R10}, t_{F10}	When using external device expansion function			160	ns
		When not using external device expansion function			1,000	ns

Note C is the load capacitance of the SO1 output line.

(iii) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK1}$...Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY11}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1,600			ns
$\overline{SCK1}$ high-/low-level width	t_{KH11}, t_{KL11}	V_{DD} = 4.5 to 5.5 V	$t_{KCY11}/2 - 50$			ns
			$t_{KCY11}/2 - 100$			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK11}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI11}		400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO11}	C = 100 pF[Note]			300	ns
STB↑ from $\overline{SCK1}$↑	t_{SBD}		$t_{KCY11}/2 - 100$		$t_{KCY11}/2 + 100$	ns
Strobe signal high-level width	t_{SBW}	2.7 V ≤ V_{DD} < 5.5 V	$t_{KCY11} - 30$		$t_{KCY11} + 30$	ns
Busy signal setup time (to busy signal detection timing)	t_{BYS}		100			ns
Busy signal hold time (from busy signal detection timing)	t_{BYH}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
$\overline{SCK1}$↓ from busy inactive	t_{SPS}				$2t_{KCY11}$	ns

Note C is the load capacitance of the $\overline{SCK1}$ and SO1 output lines.

(iv) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK1}$...External clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY12}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.7 V ≤ V_{DD} < 4.5 V		1,600			ns
$\overline{SCK1}$ high-/low-level width	t_{KH12}, t_{KL12}	4.5 V ≤ V_{DD} ≤ 5.5 V		400			ns
		2.7 V ≤ V_{DD} < 4.5 V		800			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK12}	V_{DD} = 2.7 to 5.5 V		100			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI12}			400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO12}	C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V			300	ns
$\overline{SCK1}$ rise/fall time	t_{R12}, t_{F12}	When using external device expansion function				160	ns
		When not using external device expansion function				1,000	ns

Note C is the load capacitance of the SO1 output line.

(c) Serial interface channel 2

(i) 3-wire serial I/O mode ($\overline{SCK2}$...Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY13}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1,600			ns
$\overline{SCK2}$ high-/low-level width	t_{KH13}, t_{KL13}	V_{DD} = 4.5 to 5.5 V	t_{KCY13}/2 – 50			ns
			t_{KCY13}/2 – 100			ns
SI2 setup time (to $\overline{SCK2}$↑)	t_{SIK13}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
SI2 hold time (from $\overline{SCK2}$↑)	t_{KSI13}		400			ns
SO2 output delay time from $\overline{SCK2}$↓	t_{KSO13}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of the SO2 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK2}$...External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY14}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1,600			ns
$\overline{SCK2}$ high-/low-level width	t_{KH14}, t_{KL14}	4.5 V ≤ V_{DD} ≤ 5.5 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
SI2 setup time (to $\overline{SCK2}$↑)	t_{SIK14}	V_{DD} = 2.7 to 5.5 V	100			ns
SI2 hold time (from $\overline{SCK2}$↑)	t_{KSI14}		400			ns
SO2 output delay time from $\overline{SCK2}$↓	t_{KSO14}	C = 100 pF[Note] V_{DD} = 2.7 to 5.5 V			300	ns
$\overline{SCK2}$ rise/fall time	t_{R14}, t_{F14}	Other than below			160	ns
		V_{DD} = 4.5 to 5.5 V When not using external device expansion function			1	μs

Note C is the load capacitance of the SO2 output line.

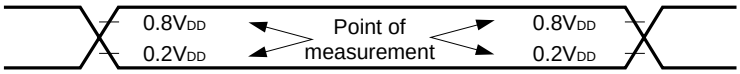
(iii) UART mode (Dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		4.5 V ≤ V_{DD} ≤ 5.5 V			78,125	bps
		2.7 V ≤ V_{DD} < 4.5 V			39,063	bps

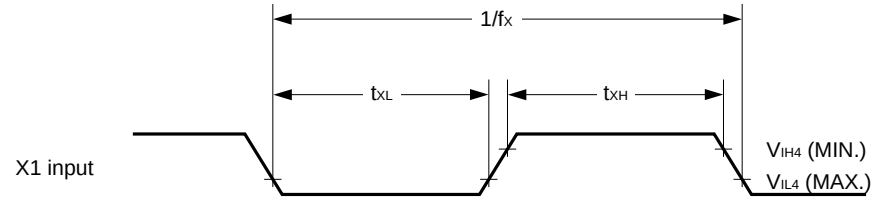
(iv) UART mode (External clock input)

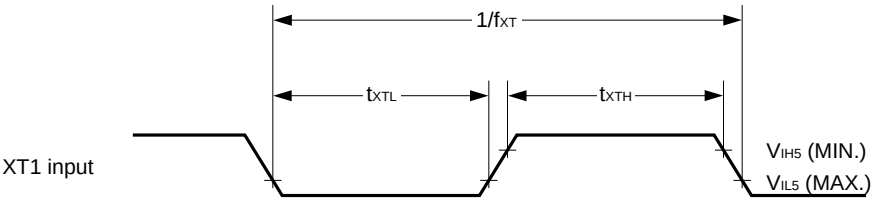
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t_{KCY15}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1,600			ns
ASCK high-/low-level width	t_{KH15}, t_{KL15}	4.5 V ≤ V_{DD} ≤ 5.5 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
Transfer rate		4.5 V ≤ V_{DD} ≤ 5.5 V			39,063	bps
		2.7 V ≤ V_{DD} < 4.5 V			19,531	bps
ASCK rise/fall time	t_{R15}, t_{F15}	V_{DD} = 4.5 to 5.5 V, when not using external device expansion function.			1,000	ns
					160	ns

AC Timing Measurement Points (Excluding X1, XT1 Inputs)

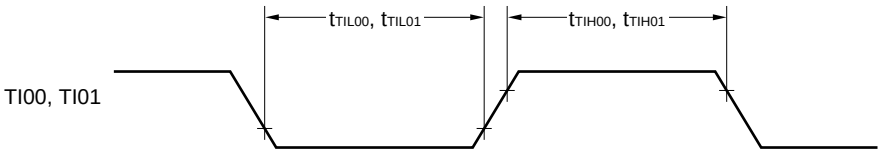


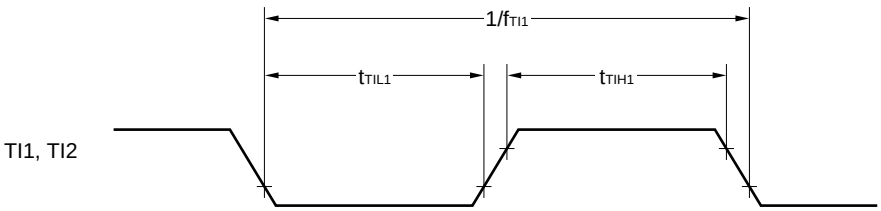
Clock Timing



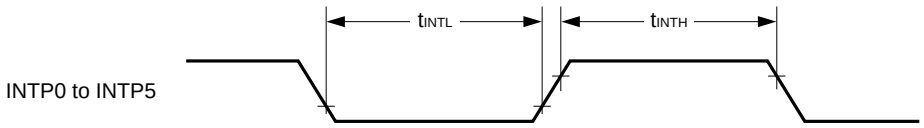


TI Timing

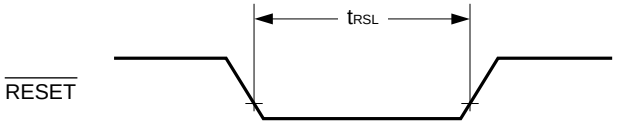




Interrupt Request Input Timing

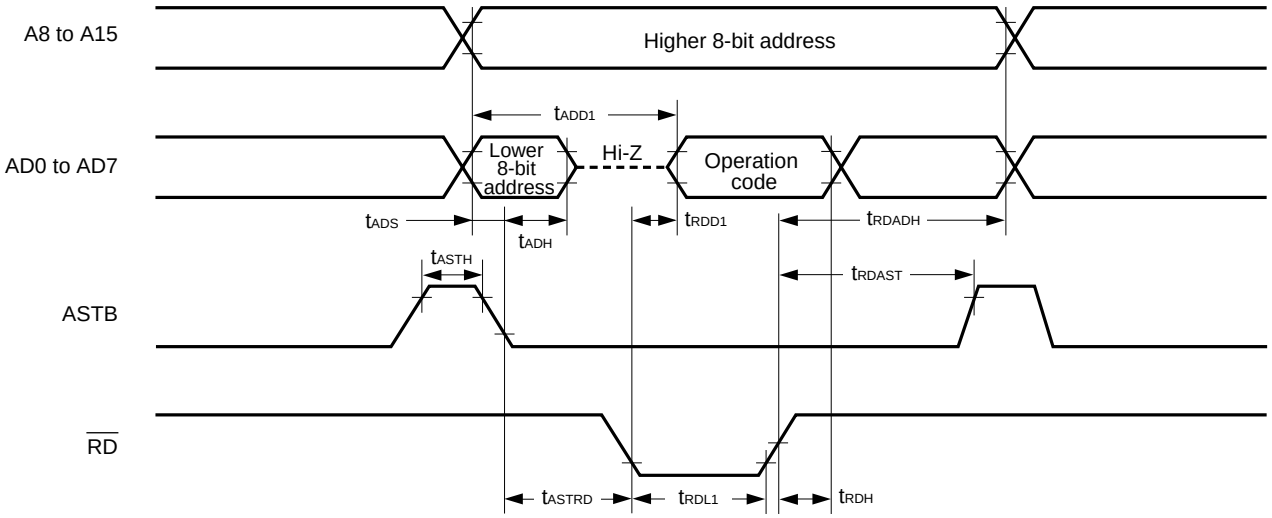


$\overline{\text{RESET}}$ Input Timing

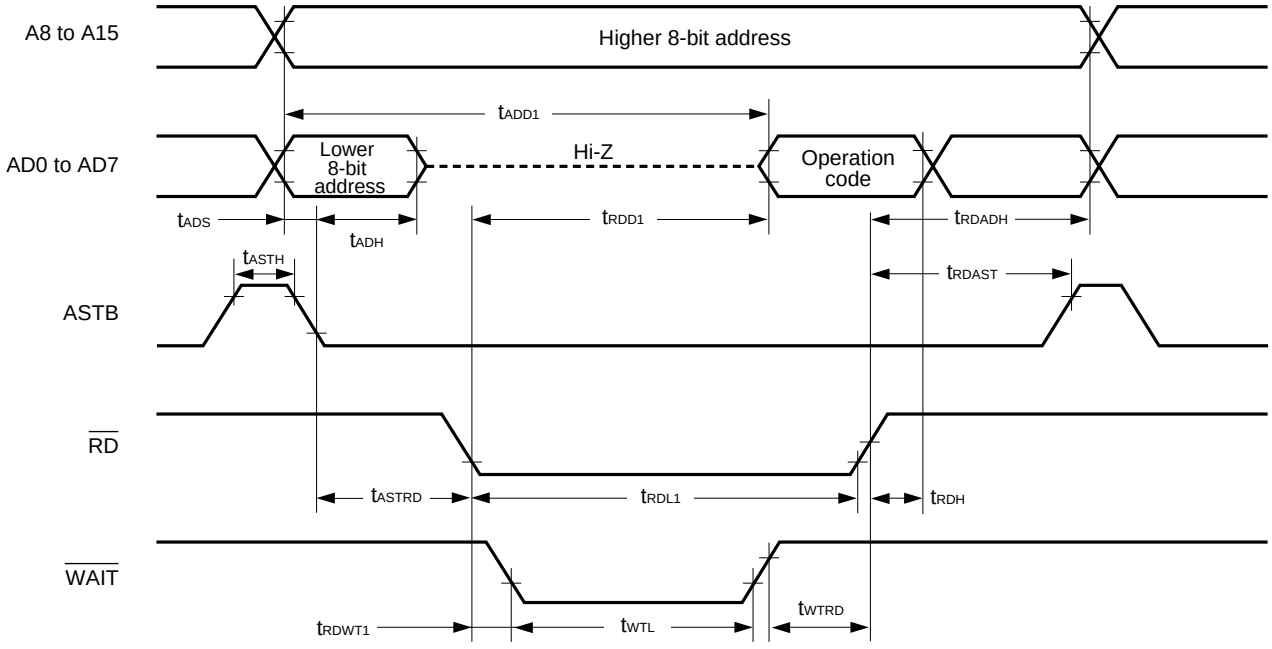


Read/Write Operation

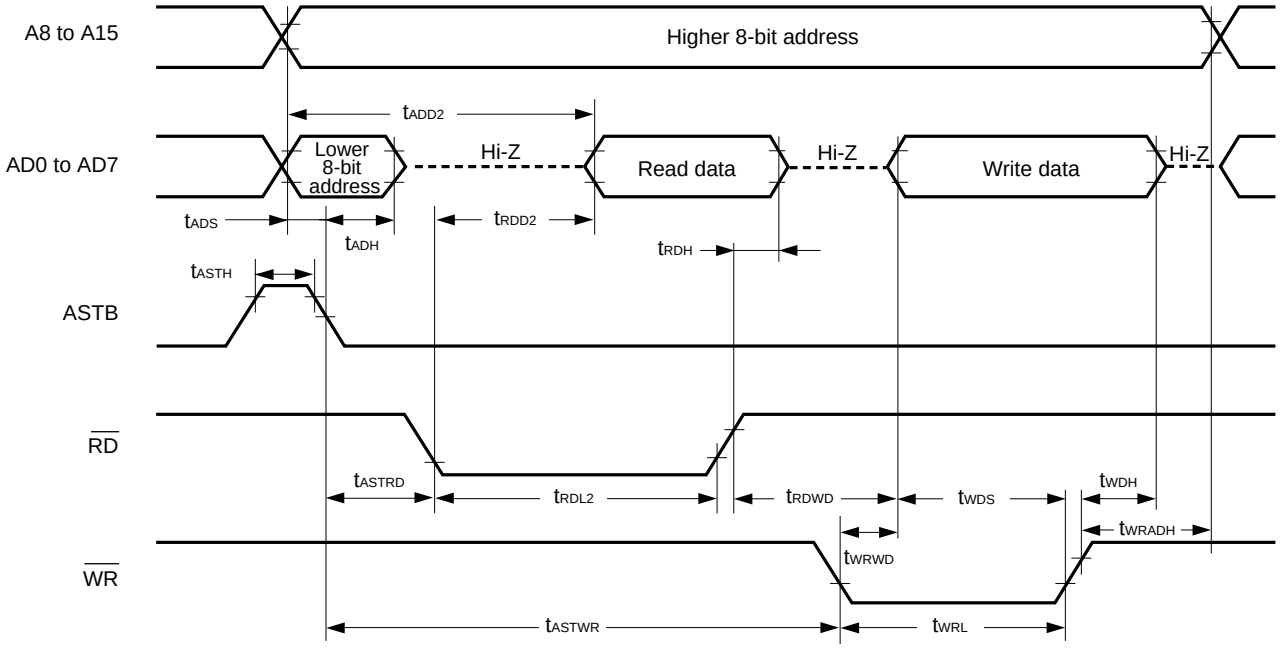
External fetch (no wait):



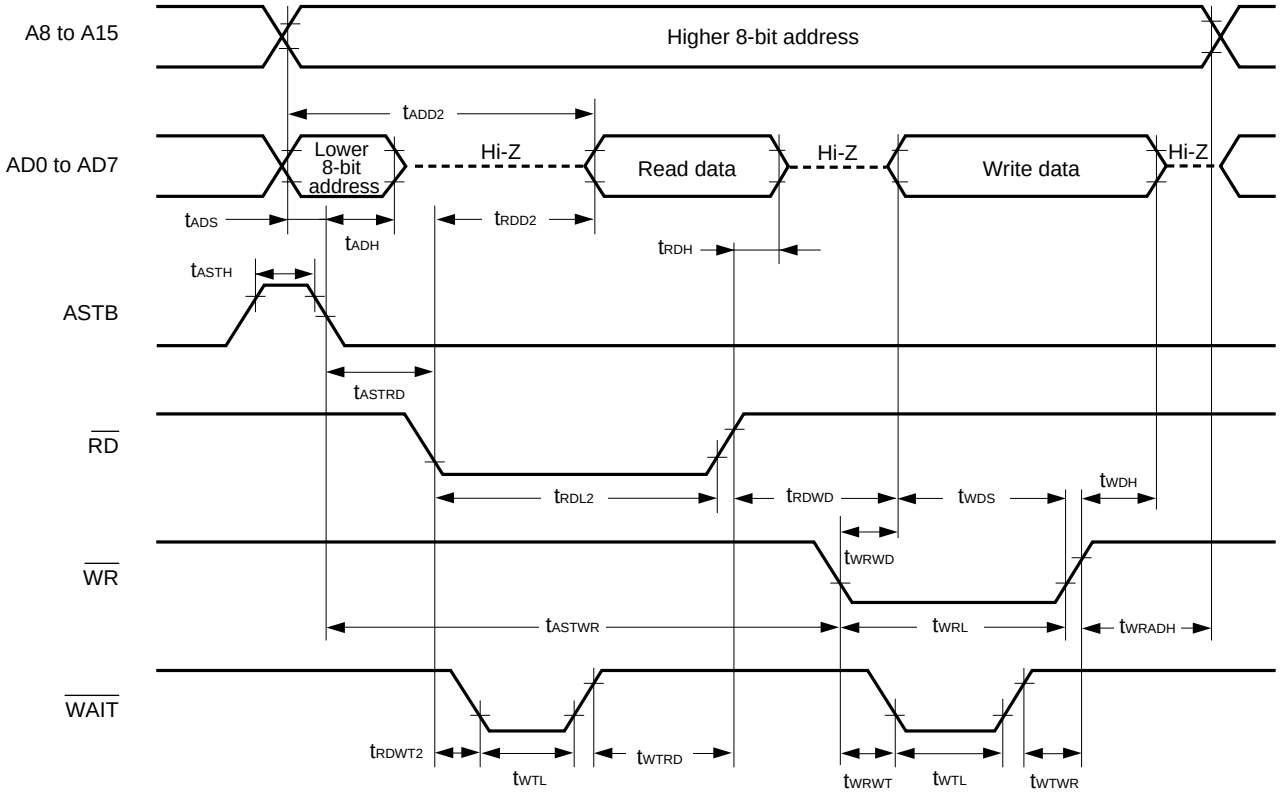
External fetch (wait insertion):



External data access (no wait):

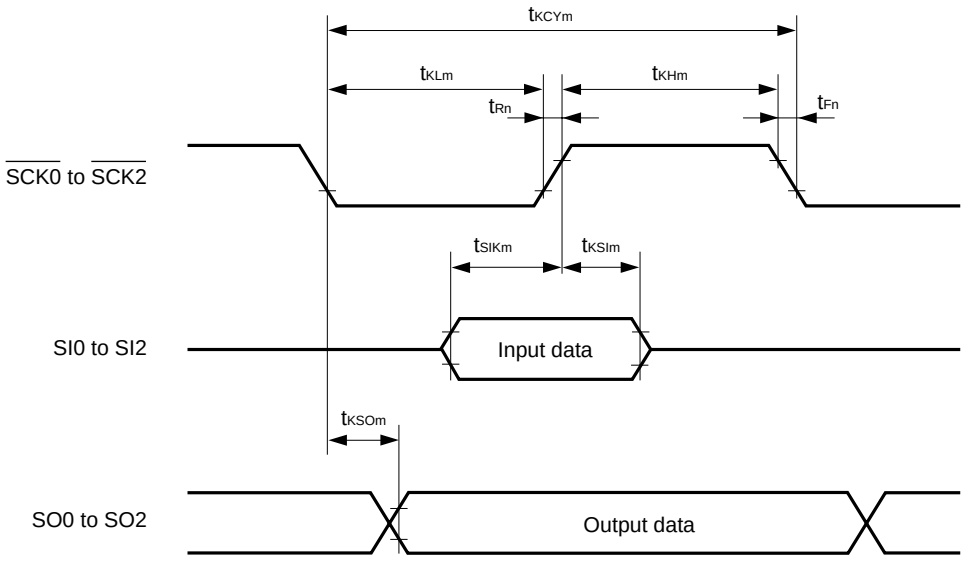


External data access (wait insertion):



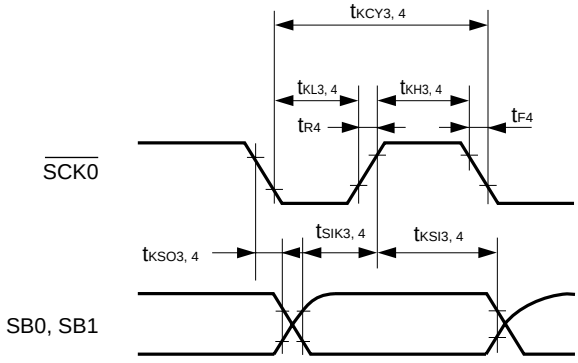
Serial Transfer Timing

3-wire serial I/O mode:

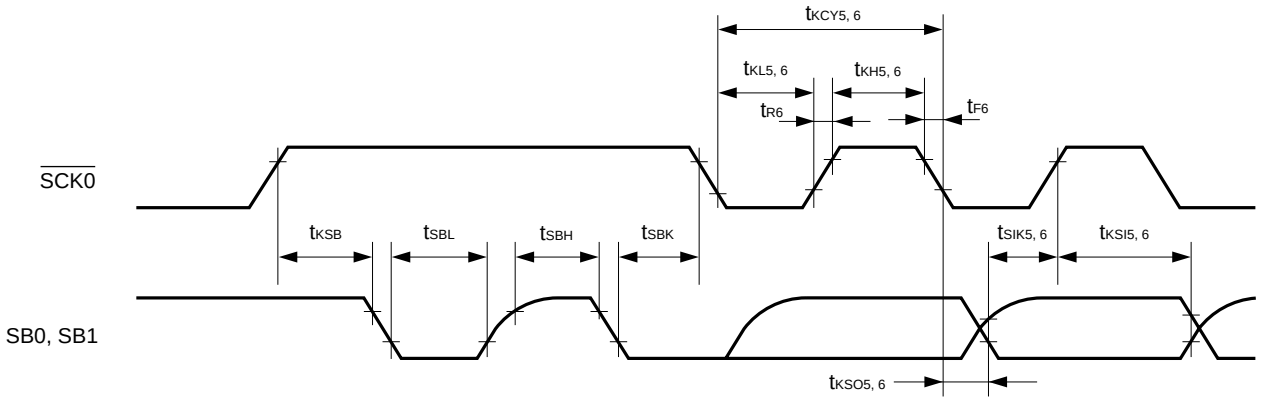


m = 1, 2, 9, 10, 13, 14
n = 2, 10, 14

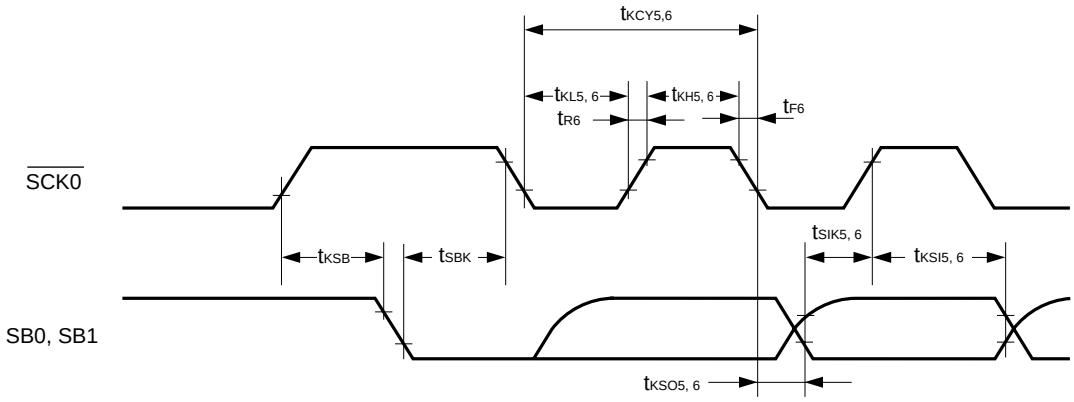
2-wire serial I/O mode:



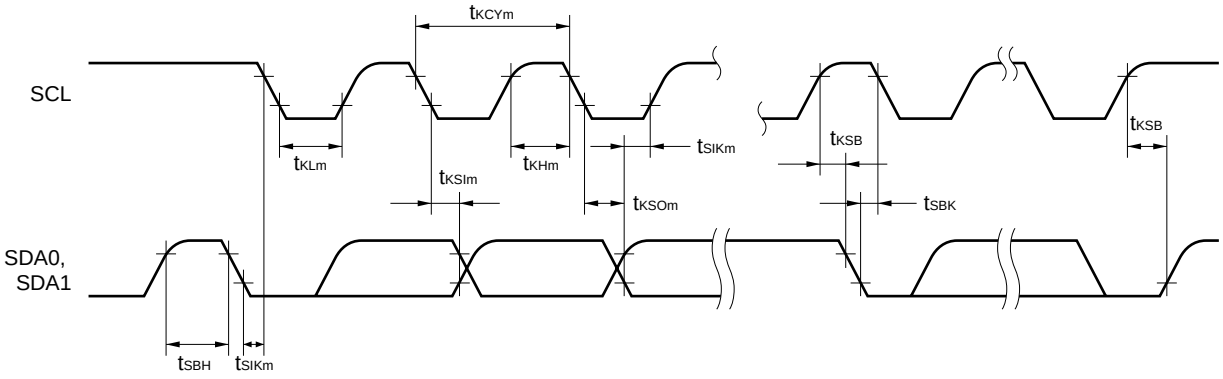
SBI mode (bus release signal transfer):



SBI mode (command signal transfer):

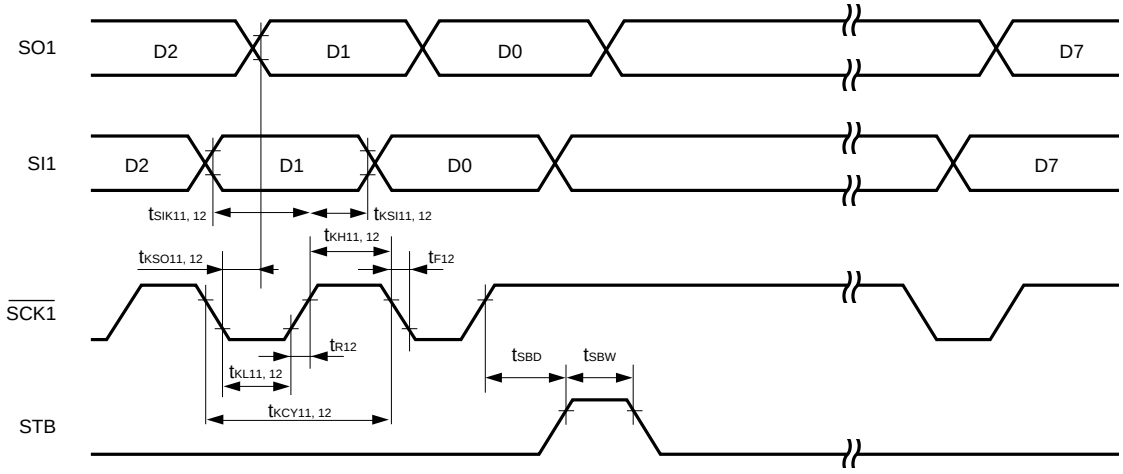


I²C bus mode :

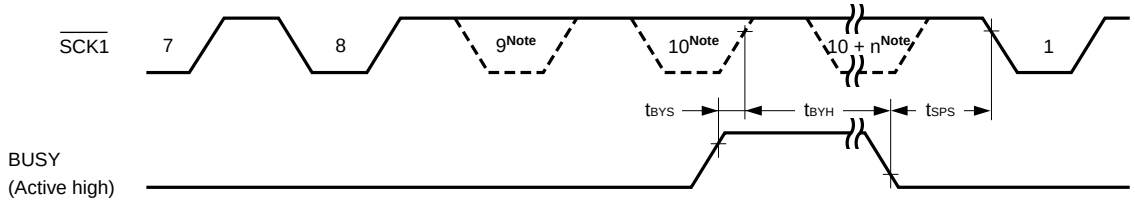


m = 7, 8

3-wire serial I/O mode with automatic transmit/receive function:

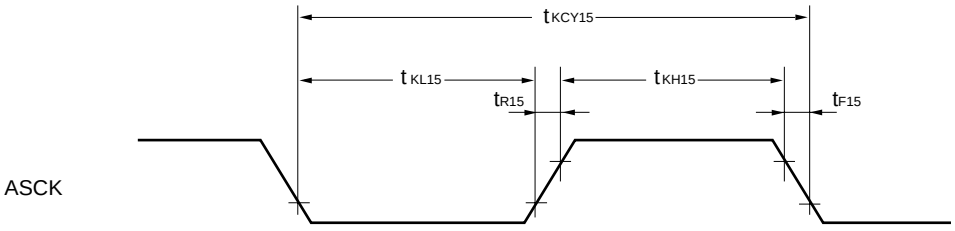


3-wire serial I/O mode with automatic transmit/receive function (busy processing):



Note The signal is not actually driven low here; it is shown as such to indicate the timing.

UART mode (external clock input):



A/D Converter Characteristics (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error[Note 1]		2.7 V ≤ AV_{REF0} < 4.5 V			±1.0	%
		4.5 V ≤ AV_{REF0} < 5.5 V			±0.6	%
Conversion time	T_{CONV}	2.7 V ≤ AV_{REF0} < 5.5 V	16		100	μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF0}	V
Reference voltage	AV_{REF0}		2.7		V_{DD}	V
AV_{REF0} current	I_{REF0}	When A/D converter is operating[Note 2]		500	1,500	μA
		When A/D converter is not operating[Note 3]		0	3	μA

Notes 1. Excludes quantization error (±1/2 LSB). This value is indicated as a ratio to the full-scale value.
2. The current flowing to the AV_{REF0} pin when bit 7 (CS) of the A/D converter mode register (ADM) is 1.
3. The current flowing to the AV_{REF0} pin when bit 7 (CS) of the A/D converter mode register (ADM) is 0.

D/A Converter Characteristics (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution					8	bit
Overall error		R = 2 MΩ[Note 1]			±1.2	%
		R = 4 MΩ[Note 1]			±0.8	%
		R = 10 MΩ[Note 1]			±0.6	%
Settling time		C = 30 pF[Note 1]			15	μs
Output resistance	R_O	**Note 2**		8		kΩ
Analog reference voltage	AV_{REF1}		1.8		V_{DD}	V
AV_{REF1} current	I_{REF1}	**Note 2**			2.5	mA
Resistance between AV_{REF1} and AV_{SS}	R_{AIREF1}	DACS0, DACS1 = 55H[Note 2]	4	8		kΩ

Notes 1. R and C are the D/A converter output pin load resistance and load capacitance, respectively.
2. Value for one D/A converter channel

Remark DACS0 and DACS1: D/A conversion value setting registers 0, 1

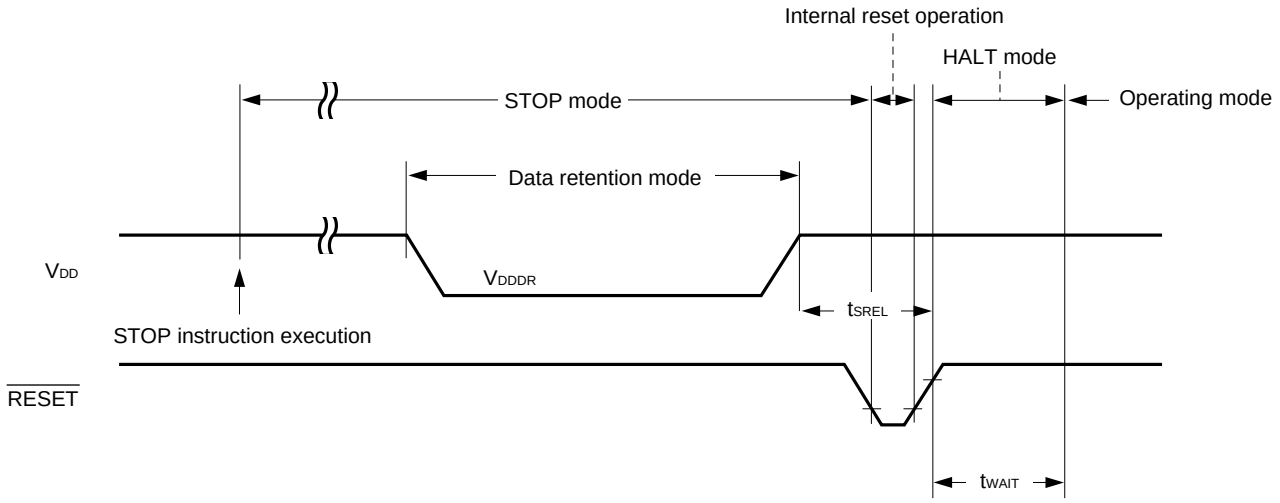
Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		1.8		5.5	V
Data retention power supply current	I_{DDDR}	V_{DDDR} = 1.8 V Subsystem clock stop and feed-back resistor disconnected		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{\text{RESET}}$		$2^{17}/f_X$		ms
		Release by interrupt request		**Note**		ms

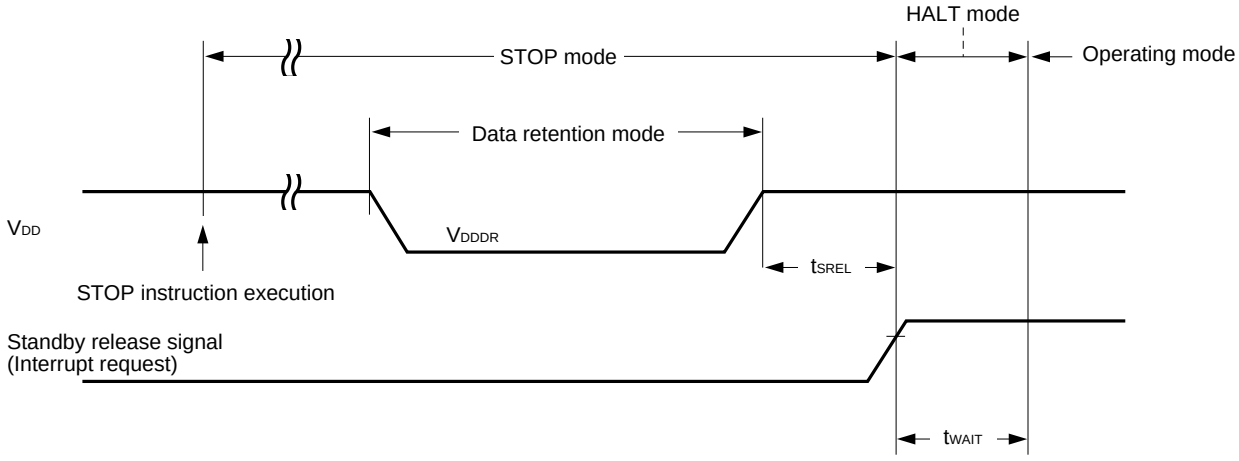
Note Selection of $2^{12}/f_{XX}$ and $2^{14}/f_{XX}$ to $2^{17}/f_{XX}$ is possible with bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).

Remark f_{XX}: Main system clock frequency (f_X or $f_X/2$)
f_X: Main system clock oscillation frequency

Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)



Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Request Signal)



Flash Memory Programming Characteristics (V_{DD} = 2.7 to 5.5 V, T_A = 10 to 40°C)

(1) Write/delete characteristics

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Write current (V_{DD} pin)Note 1	I_{DDW}	When $V_{PP} = V_{PP1}$	5.0 MHz crystal oscillation operation mode (f_{XX} = 2.5 MHz)Note 2			15.5	mA
			5.0 MHz crystal oscillation operation mode (f_{XX} = 5.0 MHz)Note 3			28.7	mA
Write current (V_{PP} pin)Note 1	I_{PPW}	When $V_{PP} = V_{PP1}$	5.0 MHz crystal oscillation operation mode (f_{XX} = 2.5 MHz)Note 2			19.5	mA
			5.0 MHz crystal oscillation operation mode (f_{XX} = 5.0 MHz)Note 3			32.7	mA
Delete current (V_{DD} pin)Note 1	I_{DDE}	When $V_{PP} = V_{PP1}$	5.0 MHz crystal oscillation operation mode (f_{XX} = 2.5 MHz)Note 2			15.5	mA
			5.0 MHz crystal oscillation operation mode (f_{XX} = 5.0 MHz)Note 3			28.7	mA
Delete current (V_{PP} pin)Note 1	I_{PPE}	When $V_{PP} = V_{PP1}$				100	mA
Unit delete time	t_{ER}			0.5	1	1	s
Total delete time	t_{ERA}					20	s
Number of overwrite	C_{WRT}	Delete and write are counted as one cycle				20	times
V_{PP} power supply voltage	V_{PP0}	In normal mode		0		0.2 V_{DD}	V
	V_{PP1}	At flash memory programming		9.7	10.0	10.3	V

Notes 1. **1.** AV_{REF} current and Port current (current flowing to internal pull-up resistor) are not included.

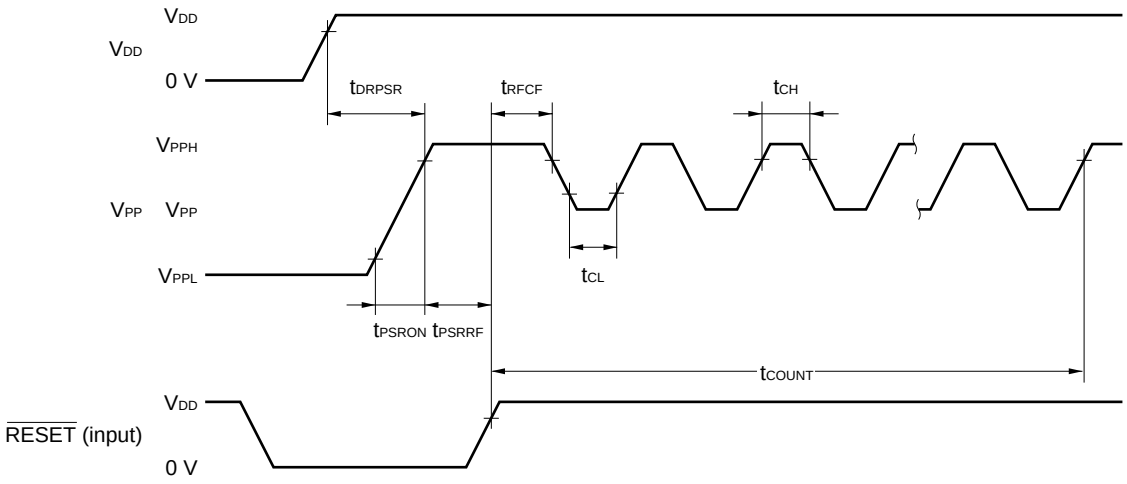
2. When main system clock is operating at $f_{XX} = f_{XX}/2$ (when oscillation mode selection resistor (OSMS) is set to 00H).

3. When main system clock is operating at $f_{XX} = f_{XX}$ (when OSMS is set to 01H).

2) Serial write operation characteristics

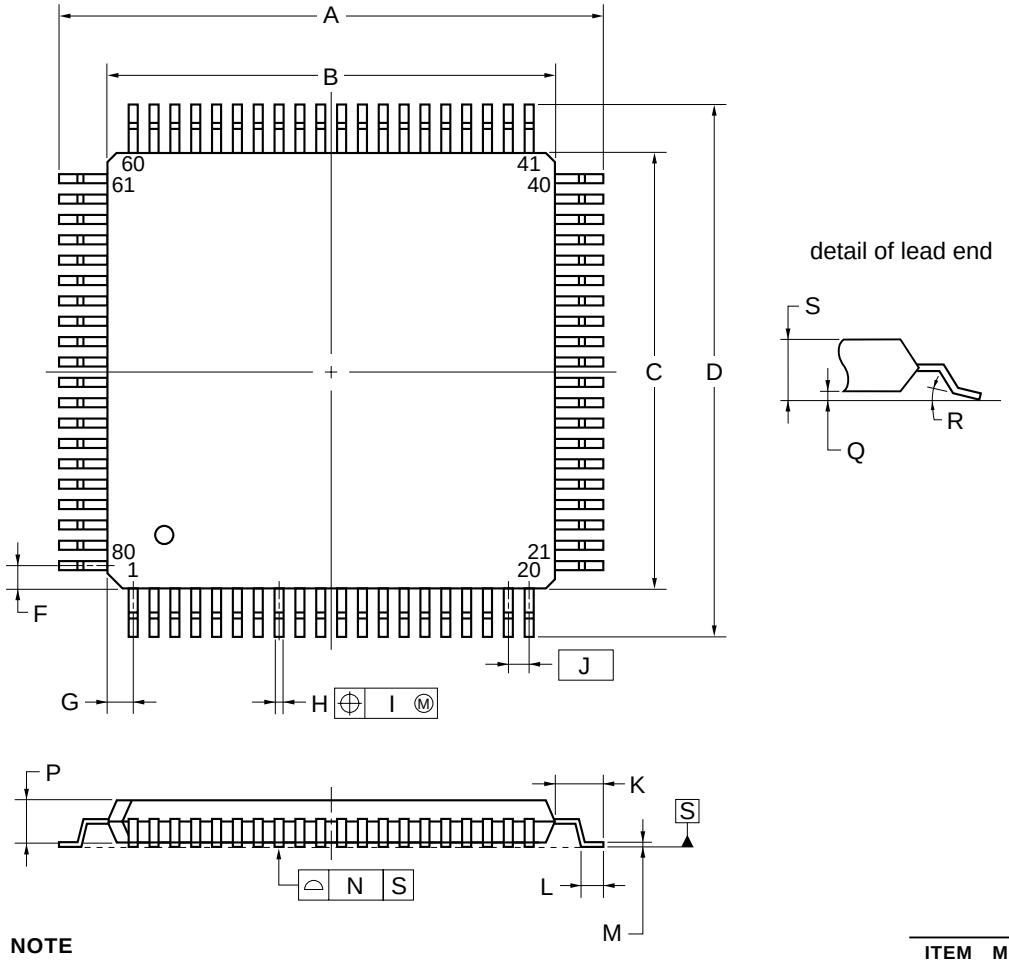
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{PP} setup time	t_{PSRON}	V_{PP} high voltage	1.0			μs
V_{PP}↑ setup time from V_{DD}↑	t_{DRPSR}	V_{PP} high voltage	1.0			μs
$\overline{RESET}$↑ setup time from V_{PP}↑	t_{PSRRF}	V_{PP} high voltage	1.0			μs
V_{PP} count start time from $\overline{RESET}$↑	t_{RFCF}		1.0			μs
Count execution time	t_{COUNT}				2.0	ms
V_{PP} counter high-level width	t_{CH}		8.0			μs
V_{PP} counter low-level width	t_{CL}		8.0			μs
V_{PP} counter noise elimination width	t_{NFW}			40		ns

Flash Write Mode Setting Timing



8. PACKAGE DRAWINGS

80-PIN PLASTIC QFP (14x14)



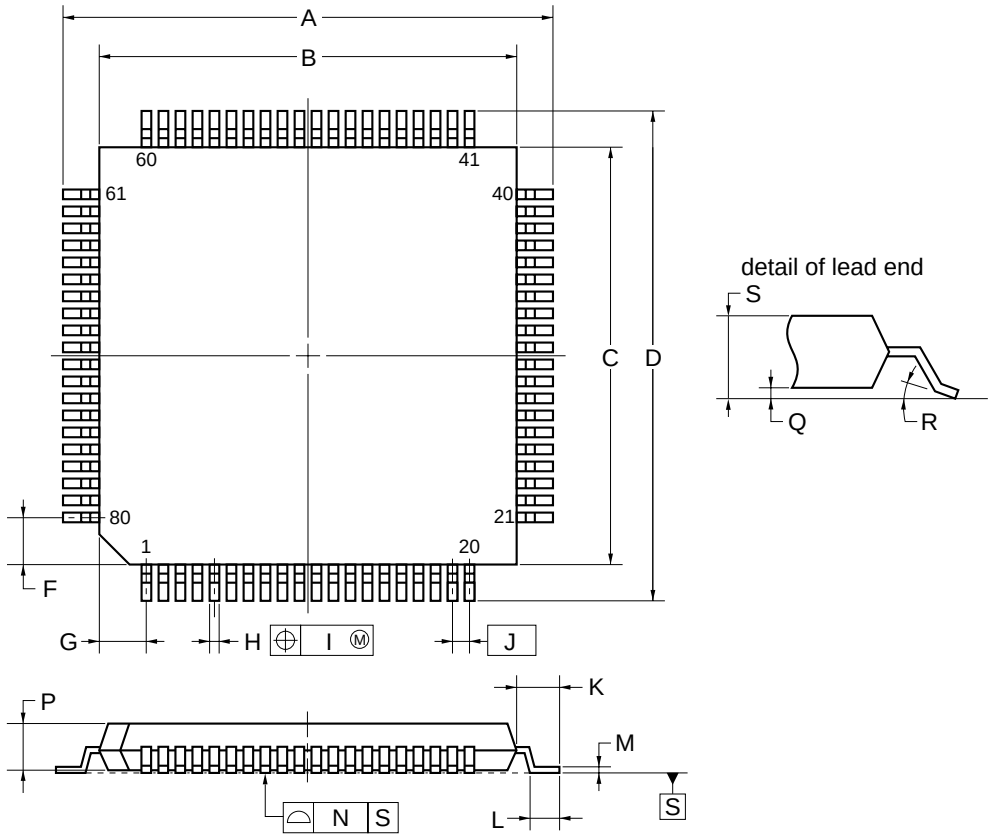
NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	17.20±0.20
B	14.00±0.20
C	14.00±0.20
D	17.20±0.20
F	0.825
G	0.825
H	0.32±0.06
I	0.13
J	0.65 (T.P.)
K	1.60±0.20
L	0.80±0.20
M	$0.17^{+0.03}_{-0.07}$
N	0.10
P	1.40±0.10
Q	0.125±0.075
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.70 MAX.

P80GC-65-8BT-1

80 PIN PLASTIC TQFP (FINE PITCH) (12x12)



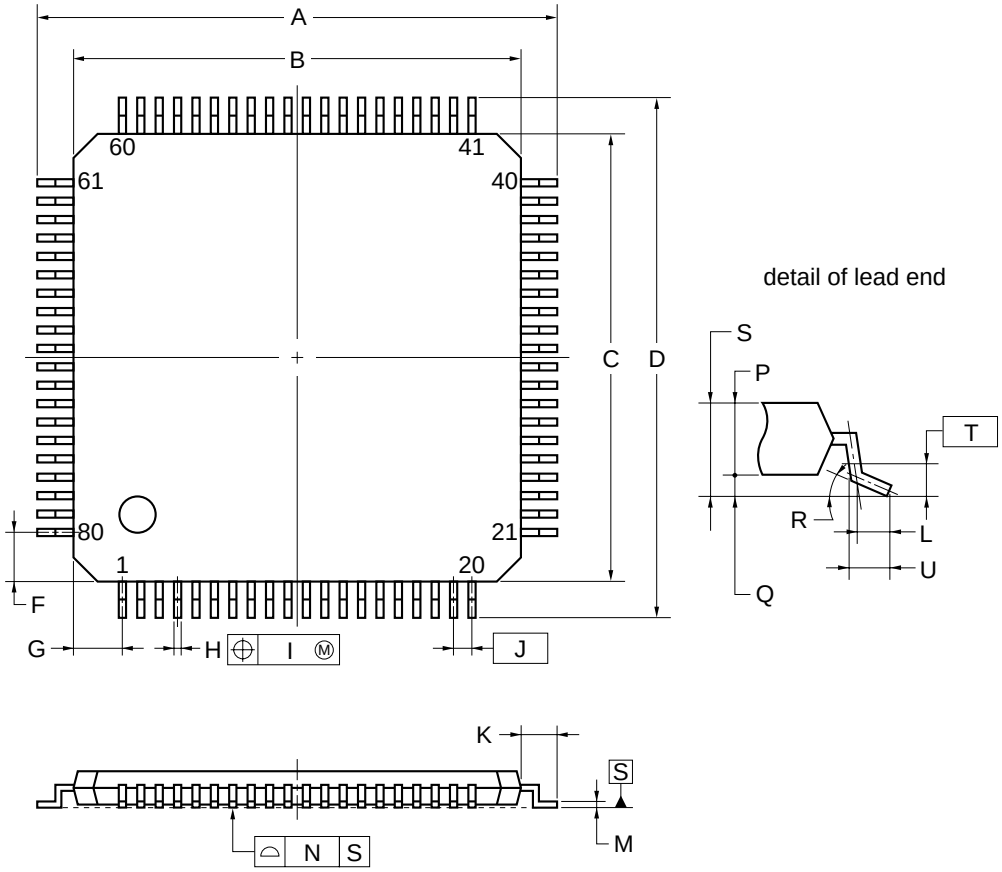
NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	14.00±0.20
B	12.00±0.20
C	12.00±0.20
D	14.00±0.20
F	1.25
G	1.25
H	$0.22^{+0.05}_{-0.04}$
I	0.10
J	0.50 (T.P.)
K	1.00±0.20
L	0.50±0.20
M	$0.145^{+0.055}_{-0.045}$
N	0.10
P	1.05±0.07
Q	0.10±0.05
R	5°±5°
S	1.27 MAX.

P80GK-50-BE9-6

★ 80-PIN PLASTIC TQFP (FINE PITCH) (12x12)



NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	14.0±0.2
B	12.0±0.2
C	12.0±0.2
D	14.0±0.2
F	1.25
G	1.25
H	0.22±0.05
I	0.08
J	0.5 (T.P.)
K	1.0±0.2
L	0.5
M	0.145±0.05
N	0.08
P	1.0
Q	0.1±0.05
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.1±0.1
T	0.25
U	0.6±0.15

P80GK-50-9EU-1

★ 9. RECOMMENDED SOLDERING CONDITIONS

The μPD78F0058 and 78F0058Y should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Table 9-1. Surface Mounting Type Soldering Conditions

μPD78F0058GC-8BT : 80-pin plastic QFP (14 × 14 mm)
μPD78F0058YGC-8BT : 80-pin plastic QFP (14 × 14 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Twice or less	IR35-00-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Twice or less	VP15-00-2
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once, Preheating temperature: 120°C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	–

Caution Do not use different soldering methods together (except for partial heating).

μPD78F0058GK-BE9: 80-pin plastic TQFP (12 × 12 mm, resin thickness 1.05 mm)
μPD78F0058YGK-BE9: 80-pin plastic TQFP (12 × 12 mm, resin thickness 1.05 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Twice or less, Exposure limit: 7 days[Note] (after 7 days, prebake at 125°C for 10 hours)	IR35-107-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Twice or less, Exposure limit: 7 days[Note] (after 7 days, prebake at 125°C for 10 hours)	VP15-107-2
Wave soldering	–	–
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

μPD78F0058GK-9EU : 80-pin plastic TQFP (12 × 12 mm, resin thickness 1.0 mm)
μPD78F0058YGK-9EU : 80-pin plastic TQFP (12 × 12 mm, resin thickness 1.0 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Undefined	Undefined
VPS	Undefined	Undefined
Wave soldering	Undefined	Undefined
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	–

★ APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD780058, 780058Y Subseries.

Also, refer to **(5) Cautions on using development tools.**

(1) Language processing software

RA78K0	Assembler package common to the 78K/0 Series
CC78K0	C compiler package common to the 78K/0 Series
DF780058	Device file for the μPD780058, 780058Y Subseries
CC78K0-L	C compiler library source file common to the 78K/0 Series

(2) Flash memory writing tools

Flashpro III (Part number: FL-PR3, PG-FL3)	Dedicated flash programmer for microcontrollers incorporating flash memory
FA-80GC-8BT FA-80GK FA-80GK-9EU	Adapter for flash memory writing

(3) Debugging tools

- **When using the IE-78K0-NS in-circuit emulator**

IE-78K0-NS	In-circuit emulator common to the 78K/0 Series
IE-70000-MC-PS-B	Power supply unit for IE-78K0-NS
IE-78K0-NS-PA	Performance board to enhance and expand the functions of the IE-78K0-NS
IE-70000-98-IF-C	Adapter used when a PC-9800 series PC (except notebook PC) is used as the host machine (C bus supported)
IE-70000-CD-IF-A	PC card and interface cable used when a PC-9800 series notebook PC is used as the host machine (PCMCIA socket supported)
IE-70000-PC-IF-C	Adapter necessary when an IBM PC/AT™-compatible is used as the host machine (ISA bus supported)
IE-70000-PCI-IF	Interface adapter necessary when using a PC with PCI bus as the host machine
IE-780308-NS-EM1	Emulation board common to the μPD780308 Subseries
NP-80GC	Emulation probe for 80-pin plastic QFP (GC-8BT type)
NP-80GK	Emulation probe for 80-pin plastic TQFP (GK-BE9, GK-9EU type)
TGK-080SDW	Conversion adapter to connect the NP-80GK and a target system board on which 80-pin plastic TQFP (GK-BE9, GK-9EU type) can be mounted
EV-9200GC-80	Socket to be mounted on a target system board made for 80-pin plastic QFP (GC-8BT type)
ID78K0-NS	Integrated debugger for IE-78K0-NS
SM78K0	System simulator common to the 78K/0 Series
DF780058	Device file for the μPD780058, 780058Y Subseries

- **When using the IE-78001-R-A in-circuit emulator**

IE-78001-R-A	In-circuit emulator common to the 78K/0 Series
IE-70000-98-IF-C	Adapter used when PC-9800 series PC (except notebook type) is used as host machine (C bus supported)
IE-70000-PC-IF-C	Interface adapter when using IBM PC/AT-compatible as the host machine (ISA bus supported)
IE-78000-R-SV3	Interface adapter and cable used when EWS is used as the host machine
IE-780308-NS-EM1 IE-780308-R-EM	Emulation board common to the μPD780308 Subseries
IE-78K0-R-EX1	Emulation probe conversion board necessary when using the IE-780308-NS-EM1 on the IE-78001-R-A.
EP-78230GC-R	Emulation probe for 80-pin plastic QFP (GC-8BT type)
EP-78054GK-R	Emulation probe for 80-pin plastic TQFP (GK-BE9, GK-9EU type)
TGK-080SDW	Conversion adapter to connect the EP-78054GK-R and a target system on which an 80-pin plastic TQFP (GK-BE9, GK-9EU type) can be mounted
EV-9200GC-80	Socket to be mounted on a target system board made for 80-pin plastic QFP (GC-8BT type)
ID78K0	Integrated debugger for IE-78001-R-A
SM78K0	78K/0 Series common system simulator
DF780058	Device file for the μPD780058, 780058Y Subseries

(4) Real-time OS

RX78K/0	Real-time OS for the 78K/0 Series
MX78K0	OS for the 78K/0 Series

(5) Cautions on using development tools

- The ID78K0-NS, ID78K0, and SM78K0 are used in combination with the DF780058.
- The CC78K0 and RX78K/0 are used in combination with the RA78K0 and DF780058.
- The FL-PR3, FA-80GC-8BT, FA-80GK, FA80GK-9EU, NP-80GC, and NP-80GK are products of Naito Densei Machida Mfg. Co., Ltd. (TEL: +81-44-822-3813). Contact an NEC distributor regarding the purchase of these products.
- TGK-080SDW is a product made by Tokyo Eletech Corp.
  For further information, contact Daimaru Kogyo, Ltd.
  Electronics Department (Tokyo) (TEL: +81-3-3820-7112)
  Electronics 2nd Department (Osaka) (TEL: +81-6-6244-6672)
- For third-party development tools, see the **Single-Chip Microcontroller Development Tool Selection Guide (U11069E)**
- The host machine and OS suitable for each software are as follows:

Host Machine [OS] / Software	PC PC-9800 Series [Japanese Windows™] IBM PC/AT-compatible [Japanese/English Windows]	EWS HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™ ,Solaris™] NEWS™ (RISC) [NEWS-OS™]
RA78K0	√Note	√
CC78K0	√Note	√
ID78K0-NS	√	–
ID78K0	√	√
SM78K0	√	–
RX78K/0	√Note	√
MX78K0	√Note	√

Note DOS-based software

★ APPENDIX B. RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

Document Name	Document No.	
	Japanese	English
μPD780058, 780058Y Subseries User's Manual	U12013J	U12013E
μPD780053, 780054, 780055, 780056, 780058 Data Sheet	U12182J	U12182E
μPD78F0058, 78F0058Y Data Sheet	U12092J	This document
78K/0 Series User's Manual - Instruction	U12326J	U12326E
78K/0 Series Instruction Table	U10903J	–
78K/0 Series Instruction Set	U10904J	–
78K/0, 78K/0S Series Flash Memory Write Application Note	U14458J	U14458E

Documents Related to Development Tools (User's Manuals)

Document Name		Document No.	
		Japanese	English
RA78K0 Assembler Package	Operation	U11802J	U11802E
	Assembly Language	U11801J	U11801E
	Structured Assembly Language	U11789J	U11789E
RA78K Series Structured Assembler Preprocessor		U12323J	EEU-1402
CC78K0 C Compiler	Operation	U11517J	U11517E
	Language	U11518J	U11518E
IE-78K0-NS		U13731J	U13731E
IE-78001-R-EM		To be prepared	To be prepared
IE-780308-NS-EM1		To be prepared	To be prepared
IE-780308-R-EM		U11362J	U11362E
EP-78230		EEU-985	EEU-1515
EP-78054GK-R		U13630J	–
SM78K0 System Simulator Windows Based	Reference	U10181J	U10181E
SM78K Series System Simulator	External Part User Open Interface Specifications	U10092J	U10092E
ID78K0-NS Integrated Debugger Windows Based	Reference	U12900J	U12900E
ID78K0 Integrated Debugger EWS Based	Reference	U11151J	–
ID78K0 Integrated Debugger PC Based	Reference	U11539J	U11539E
ID78K0 Integrated Debugger Windows Based	Guide	U11649J	U11649E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

Documents Related to Embedded Software (User's Manuals)

Document Name		Document No.	
		Japanese	English
78K/0 Series Real-Time OS	Fundamentals	U11537J	U11537E
	Installation	U11536J	U11536E
78K/0 Series OS MX78K0	Fundamental	U12257J	U12257E

Other Related Documents

Document Name	Document No.	
	Japanese	English
SEMICONDUCTORS SELECTION GUIDE Products & Packages (CD-ROM)	X13769X	
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Devices	C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892J	C11892E
Guide to Microcomputer-Related Products by Third Party	U11416J	–

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Purchase of NEC I^2C components conveys a license under the Philips I^2C Patent Rights to use these components in an I^2C system, provided thst the system conforms to the I^2C Standard Specification as defined by Philips.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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800-366-9782
Fax: 408-588-6130
800-729-9288

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Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

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Milton Keynes, UK
Tel: 01908-691-133
Fax: 01908-670-290

NEC Electronics Italiana s.r.l.
Milano, Italy
Tel: 02-66 75 41
Fax: 02-66 75 42 99

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  - Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
  - Specific: Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

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