DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD78F9046

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD78F9046 is a μPD789046 Subseries product (small-scale package, general-purpose applications) of the 78K/0S Series.

The μPD78F9046 has flash memory in place of the internal ROM of the μPD789046.

Because flash memory allows the program to be written and erased with the device mounted on the target board, this product is ideal for development trials, small-scale production, or for applications that require frequent upgrades.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD789046 Subseries User's Manual: U13600E
78K/0S Series User's Manual — Instruction: U11047E

FEATURES

- Pin-compatible with mask ROM version (except V_{PP} pin)
- Flash memory: 16 Kbytes
- Internal high-speed RAM: 512 bytes
- Minimum instruction execution time can be changed from high-speed (0.4 μs; @5.0-MHz operation with main system clock) to ultra-low-speed (122 μs: @32.768-kHz operation with subsystem clock)
- I/O ports: 34
- Serial interface: 1 channel
  3-wire serial I/O mode/UART mode can be selected
- Timer: 4 channels
  - 16-bit timer: 1 channel
  - 8-bit timer/event counter: 1 channel
  - Watch timer: 1 channel
  - Watchdog timer: 1 channel
- Power supply voltage: V_{DD} = 1.8 to 5.5 V

APPLICATIONS

Cordless phones, etc.

ORDERING INFORMATION

	Part Number	Package
★	μPD78F9046GB-8ES	44-pin plastic LQFP (10 × 10 mm)

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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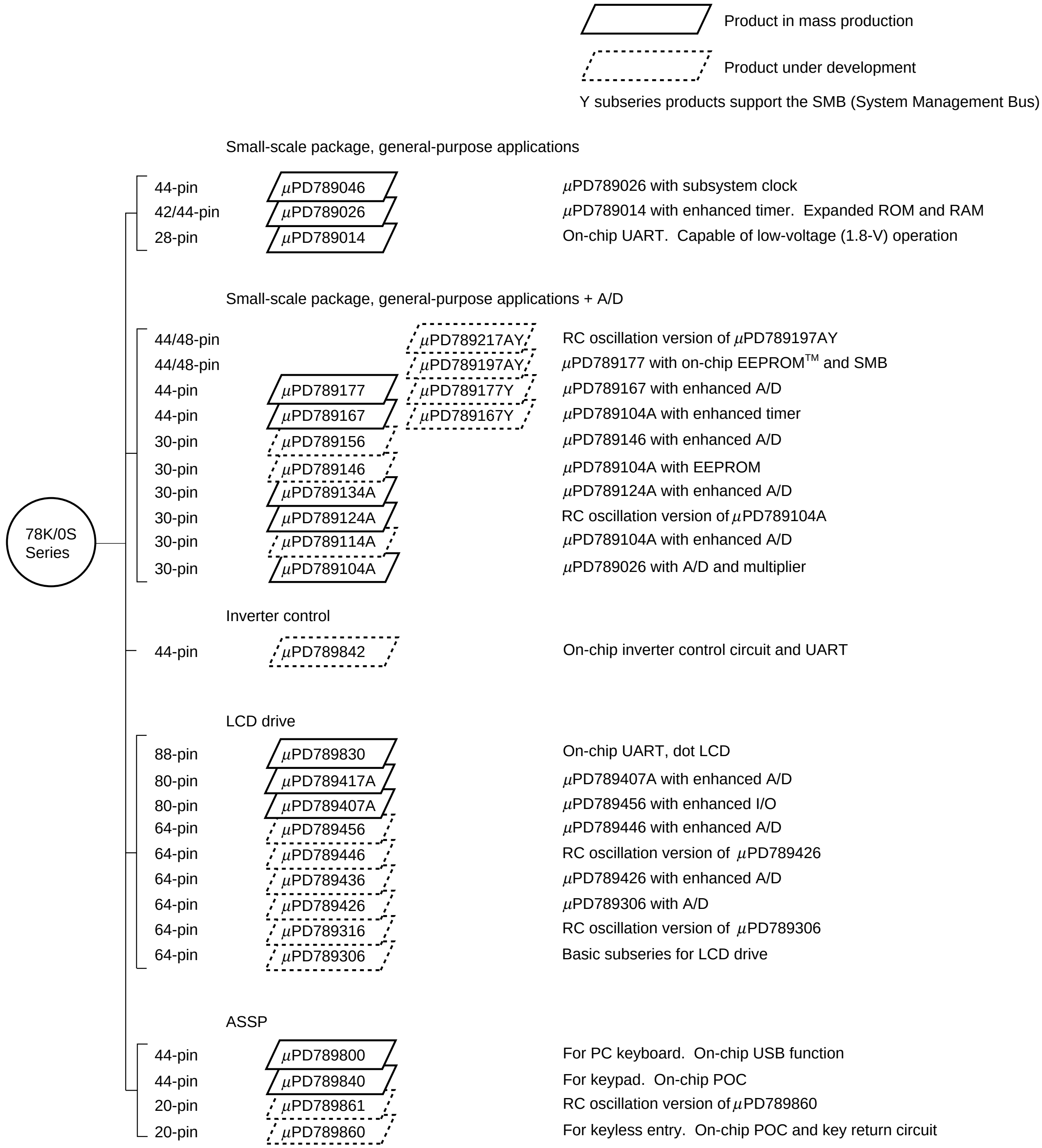
The mark ★ shows revised points.

★ 78K/0S SERIES LINEUP

The products in the 78K/0S Series are listed below. The names enclosed in boxes are subseries names.



The major functional differences among the subseries are listed below.

Subseries Name (Function)		ROM Capacity	Timer 8-bit	Timer 16-bit	Timer Watch	Timer WDT	8-Bit A/D	10-Bit A/D	Serial Interface	I/O	V_{DD} MIN. Value	Remark
Small-scale package, general-purpose applications	μPD789046	16 K	1 ch	1 ch	1 ch	1 ch	—	—	1 ch (UART:1 ch)	34	1.8 V	—
	μPD789026	4 K to 16 K			—							
	μPD789014	2 K to 4 K	2 ch	—						22		
Small-scale package, general-purpose applications + A/D	μPD789177	16 K to 24 K					—	8 ch	1 ch (UART: 1 ch)	31		—
	μPD789167						8 ch	—				
	μPD789156	8 K to 16 K	1 ch		—		—	4 ch		20		On-chip EEPROM
	μPD789146						4 ch	—				
	μPD789134A	2 K to 8 K					—	4 ch				RC oscillation version
	μPD789124A						4 ch	—				
	μPD789114A						—	4 ch				—
	μPD789104A						4 ch	—				
Inverter control	μPD789842	8 K to 16 K	3 ch	**Note**	1 ch	1 ch	8 ch	—	1 ch (UART: 1 ch)	30	4.0 V	—
LCD drive	μPD789830	24 K	1 ch	1 ch	1 ch	1 ch	—	—	1 ch (UART: 1 ch)	30	2.7 V	—
	μPD789417A	12 K to 24 K	3 ch					7 ch		43	1.8 V	
	μPD789407A						7 ch	—				
	μPD789456	12 K to 16 K	2 ch				—	6 ch	1 ch (UART: 1 ch)	30		
	μPD789446						6 ch	—				
	μPD789436						—	6 ch		40		
	μPD789426						6 ch	—				
	μPD789316	8 K to 16 K					—		2 ch (UART: 1 ch)	23		RC oscillation version
	μPD789306											—
ASSP	μPD789800	8 K	2 ch	1 ch	—	1 ch	—	—	2 ch (USB: 1 ch)	31	4.0 V	—
	μPD789840						4 ch		1 ch	29	2.8 V	
	μPD789861	4 K		—			—		—	14	1.8 V	RC oscillation version
	μPD789860											—

Note 10-bit timer: 1 channel

OVERVIEW OF FUNCTIONS

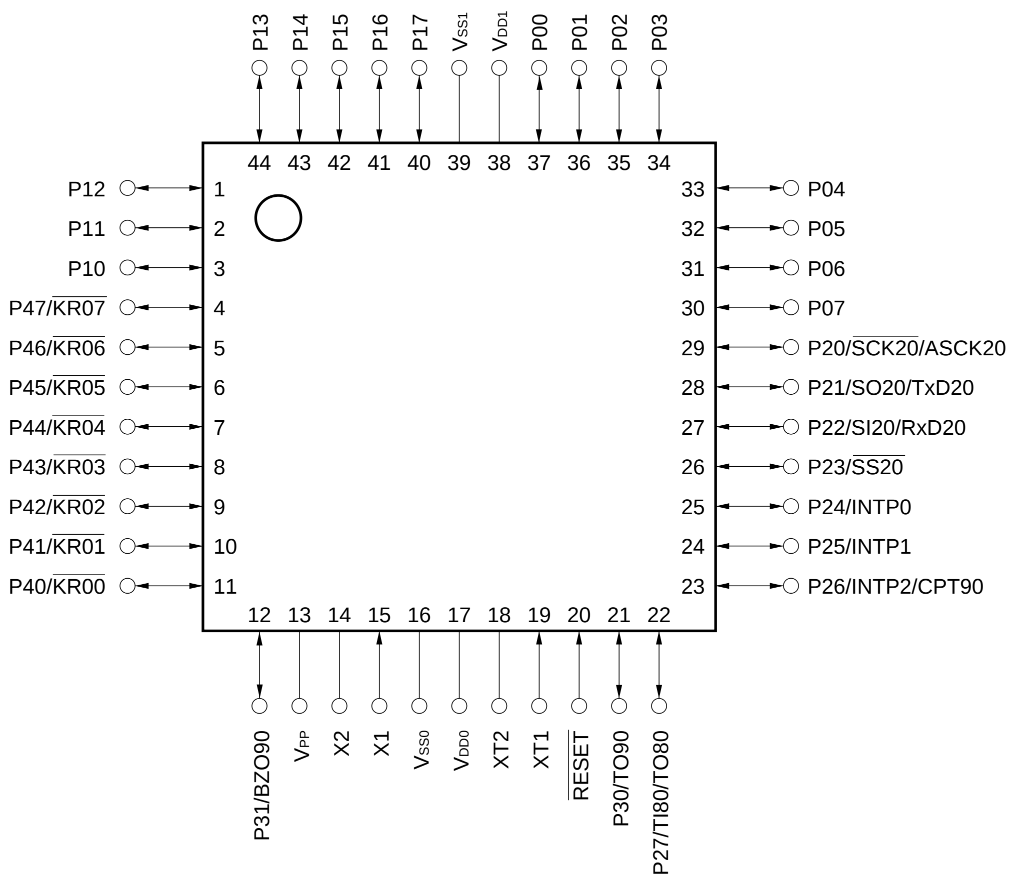
Item		Function
Internal memory	Flash memory	16 Kbytes
	High-speed RAM	512 bytes
Minimum instruction execution time		0.4 μs/1.6 μs (@ 5.0-MHz operation with main system clock) 122 μs (@32.768-kHz operation with subsystem clock)
General-purpose registers		8 bits × 8 registers
Instruction set		• 16-bit operation • Bit manipulation (set, reset, test), etc.
I/O ports		• CMOS I/O: 34
Serial interface		• 3-wire serial I/O mode/UART mode selectable: 1 channel
Timer		• 16-bit timer: 1 channel • 8-bit timer/event counter: 1 channel • Watch timer: 1 channel • Watchdog timer: 1 channel
Timer outputs		2
Vectored interrupt sources	Maskable	Internal: 7, External: 4
	Non-maskable	Internal: 1
Power supply voltage		V_{DD} = 1.8 to 5.5 V
Operating ambient temperature		T_A = –40 to +85°C
★ Package		44-pin plastic LQFP (10 × 10 mm)

CONTENTS

1. PIN CONFIGURATION (TOP VIEW)

- **44-pin plastic LQFP (10 × 10 mm)**

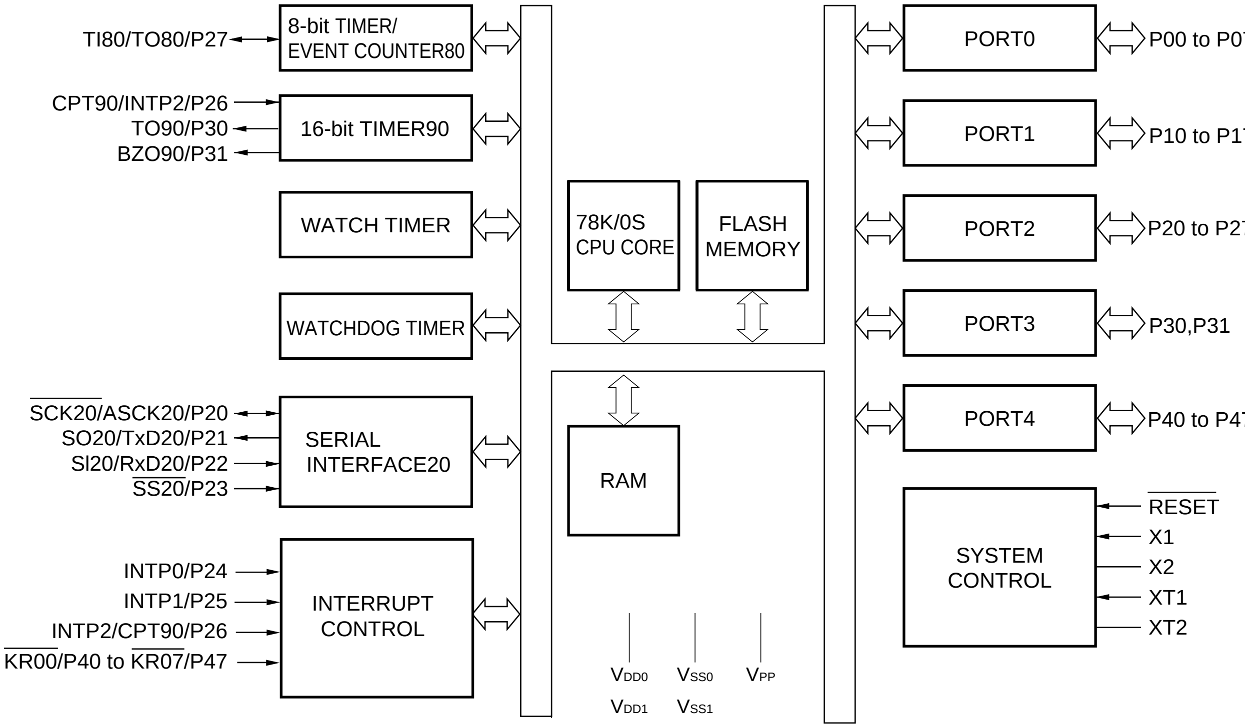
  μPD78F9046GB-8ES



Caution Connect the V_{PP} pin directly to V_{SS0} or V_{SS1} in normal operation mode.

ASCK20:	Asynchronous Serial Input	$\overline{SCK20}$:	Serial Clock
BZO90:	Buzzer Output	SI20:	Serial Input
CPT90:	Capture Trigger Input	SO20:	Serial Output
INTP0 to INTP2:	Interrupt from Peripherals	$\overline{SS20}$:	Chip Select Input
$\overline{KR00}$ to $\overline{KR07}$:	Key Return	TI80:	Timer Input
P00 to P07:	Port 0	TO80, TO90:	Timer Output
P10 to P17:	Port 1	TxD20:	Transmit Data
P20 to P27:	Port 2	V_{DD0}, V_{DD1}:	Power Supply
P30, P31:	Port 3	V_{PP}:	Programming Power Supply
P40 to P47:	Port 4	V_{SS0}, V_{SS1}:	Ground
$\overline{RESET}$:	Reset	X1, X2:	Crystal (Main System Clock)
RxD20:	Receive Data	XT1, XT2:	Crystal (Subsystem Clock)

2. BLOCK DIAGRAM



3. PIN FUNCTIONS

3.1 Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
P00 to P07	I/O	Port 0 8-bit input/output port Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.	Input	—
P10 to P17	I/O	Port 1 8-bit input/output port Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.	Input	—
P20	I/O	Port 2 8-bit input/output port Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.	Input	$\overline{\text{SCK20}}$/ASCK20
P21				SO20/TxD20
P22				SI20/RxD20
P23				$\overline{\text{SS20}}$
P24				INTP0
P25				INTP1
P26				INTP2/CPT90
P27				TI80/TO80
P30	I/O	Port 3 2-bit input/output port Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.	Input	TO90
P31				BZO90
P40 to P47	I/O	Port 4 8-bit input/output port Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.	Input	$\overline{\text{KR00}}$ to $\overline{\text{KR07}}$

3.2 Non-Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.	Input	P24
INTP1				P25
INTP2				P26/CPT90
$\overline{\text{KR00}}$ to $\overline{\text{KR07}}$	Input	Key return signal detection	Input	P40 to P47
SI20	Input	Serial interface serial data input	Input	P22/RxD20
SO20	Output	Serial interface serial data output	Input	P21/TxD20
$\overline{\text{SCK20}}$	I/O	Serial interface serial clock input/output	Input	P20/ASCK20
$\overline{\text{SS20}}$	Input	Chip select input for serial interface	Input	P23
ASCK20	Input	Serial clock input for asynchronous serial interface	Input	P20/$\overline{\text{SCK20}}$
RxD20	Input	Serial data input for asynchronous serial interface	Input	P22/SI20
TxD20	Output	Serial data output for asynchronous serial interface	Input	P21/SO20
TI80	Input	External count clock input to 8-bit timer 80	Input	P27/TO80
TO80	Output	8-bit timer 80 output	Input	P27/TI80
TO90	Output	16-bit timer 90 output	Input	P30
BZO90	Output	16-bit timer 90 buzzer output	Input	P31
CPT90	Input	Capture edge input	Input	P26/INTP2
X1	Input	Connecting crystal resonator for main system clock oscillation	–	–
X2	–		–	–
XT1	Input	Connecting crystal resonator for subsystem clock oscillation	–	–
XT2	–		–	–
V_{DD0}	–	Positive power supply of ports	–	–
V_{DD1}	–	Positive power supply (except ports)	–	–
V_{SS0}	–	Ground potential of ports	–	–
V_{SS1}	–	Ground potential (except ports)	–	–
$\overline{\text{RESET}}$	Input	System reset input	Input	–
V_{PP}	–	Flash memory programming mode setting. High-voltage application for program write/verify. Connect directly to V_{SS0} or V_{SS1} in normal operation mode.	–	–

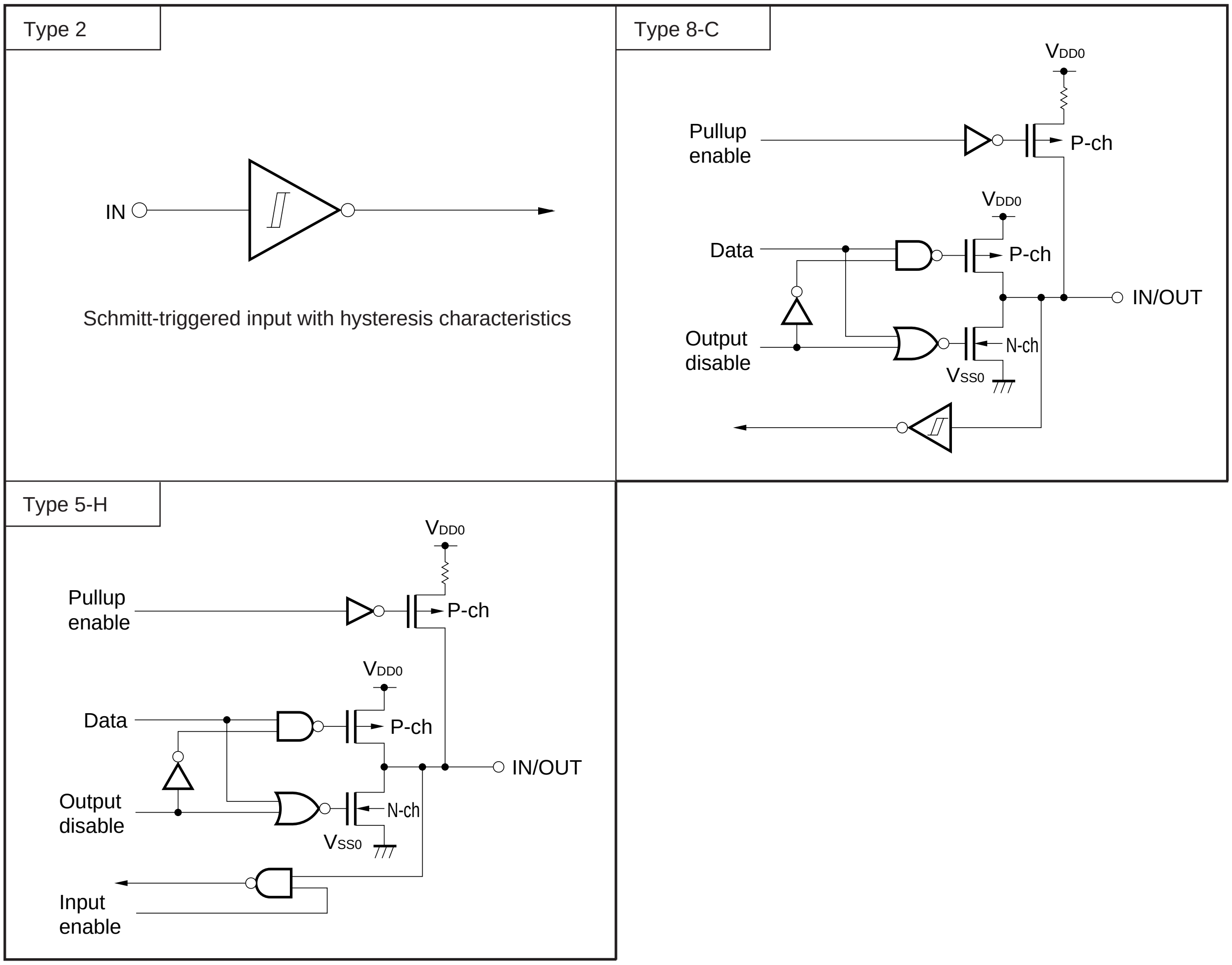
3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 3-1.
For the input/output circuit configuration of each type, refer to Figure 3-1.

Table 3-1. Types of Input/Output Circuits and Recommended Connection of Unused Pins

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00 to P07	5-H	I/O	Input: Independently connect to V_{DD0} or V_{DD1}, or V_{SS0} or V_{SS1} via a resistor. Output: Leave open.
P10 to P17			
P20/$\overline{SCK20}$/ASCK20	8-C		
P21/SO20/TxD20			
P22/SI20/RxD20			
P23/$\overline{SS20}$			
P24/INTP0			
P25/INTP1			
P26/INTP2/CPT90			
P27/TI80/TO80			
P30/TO90	5-H		
P31/BZO90			
P40/$\overline{KR00}$ to P47/$\overline{KR07}$	8-C		
XT1	–	Input	Connect to V_{SS0} or V_{SS1}.
XT2		–	Leave open.
$\overline{RESET}$	2	Input	–
V_{PP}	–	–	Connect directly to V_{SS0} or V_{SS1}.

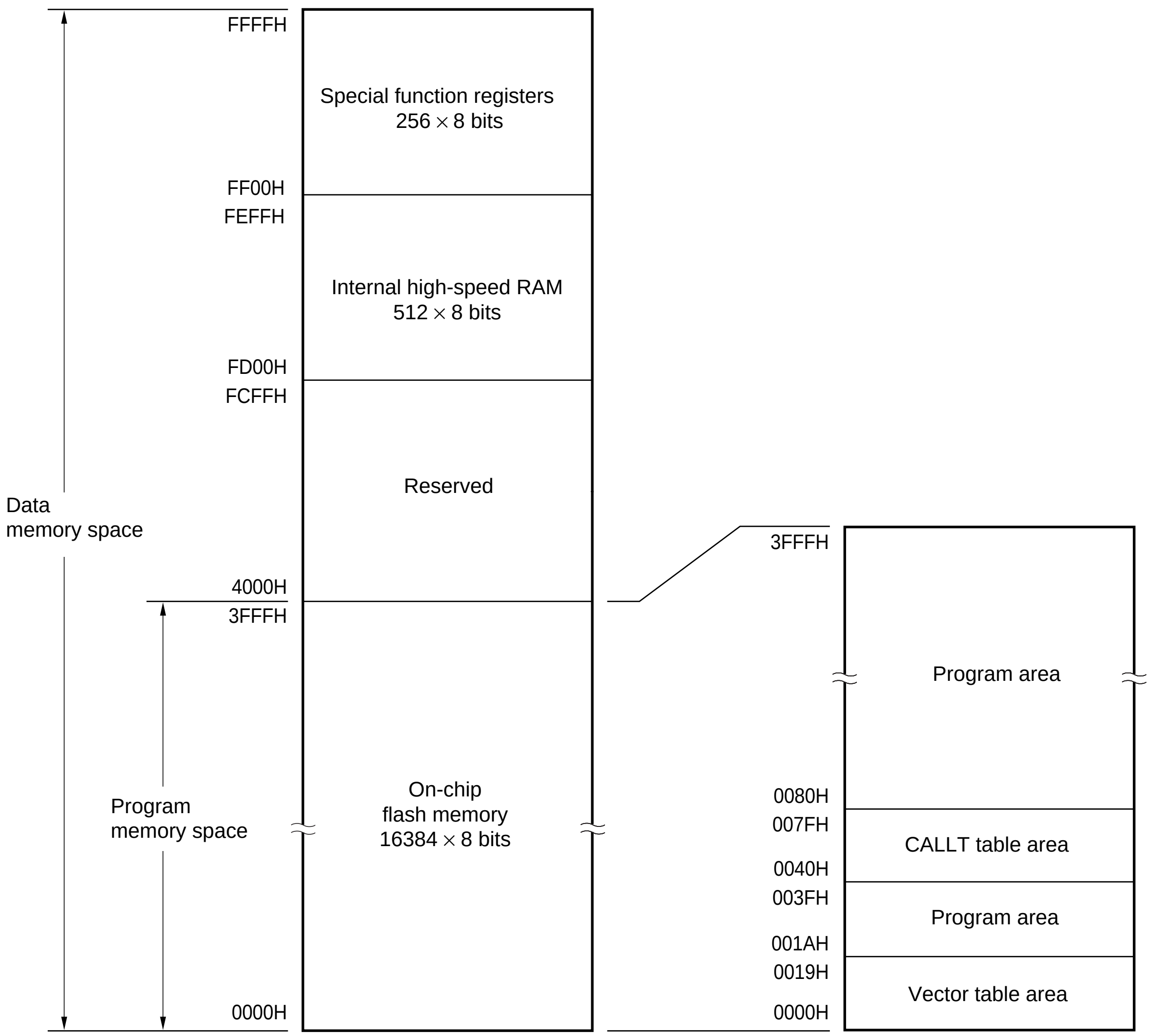
Figure 3-1. Pin Input/Output Circuits



4. MEMORY SPACE

The μPD78F9046 can access up to 64 Kbytes of memory space. Figure 4-1 shows the memory map.

Figure 4-1. Memory Map



5. PROGRAMMING FLASH MEMORY

The program memory that is incorporated in the μPD78F9046 is flash memory.

With flash memory, it is possible to write programs on-board. Writing is performed by connecting a dedicated flash programmer (Flashpro III, (Part No. FL-PR3, PG-FP3)) to the host machine and the target system.

Remark FL-PR3 is a product of Naito Densei Machida Mfg. Co., Ltd.

5.1 Selecting Communication Mode

Writing to flash memory is performed using the Flashpro III in a serial communication mode. Select one of the communication modes in Table 5-1. The selection of the communication mode is made by using the format shown in Figure 5-1. Each communication mode is selected using the number of V_{PP} pulses shown in Table 5-1.

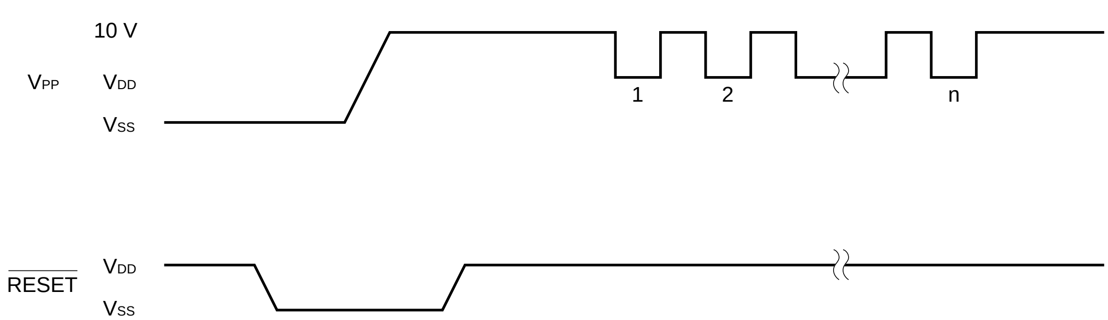
Table 5-1. List of Communication Mode

Communication Mode	Pins	V_{PP} Pulses
3-wire serial I/O	$\overline{\text{SCK20}}$/ASCK20/P20 SO20/TxD20/P21 SI20/RxD20/P22	0
UART	TxD20/SO20/P21 RxD20/SI20/P22	8
Pseudo 3-wire[Note]	P00 (Serial clock input) P01 (Serial data output) P02 (Serial data input)	12

Note Serial transfer is carried out by controlling ports with software.

Caution Be sure to select a communication mode using the number of V_{PP} pulses shown in Table 5-1.

Figure 5-1. Format of Communication Mode Selection



5.2 Function of Flash Memory Programming

Operations such as writing to flash memory are performed by various command/data transmission and reception operations according to the selected communication mode. Table 5-2 shows the major functions of flash memory programming.

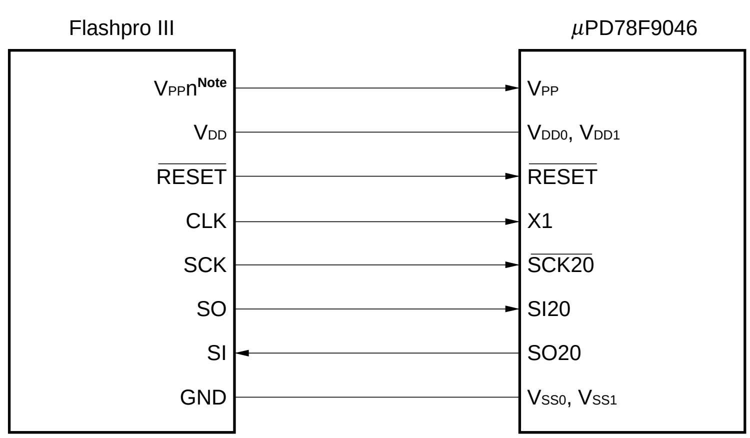
Table 5-2. Major Function of Flash Memory Programming

Function	Description
Batch erase	Deletes the entire memory contents
Batch blank check	Checks the deletion status of the entire memory
Data write	Performs a write operation to the flash memory based on the write start address and the number of data to be written (number of bytes).
Batch verify	Compares the entire memory contents with the input data.

5.3 Connecting Flashpro III

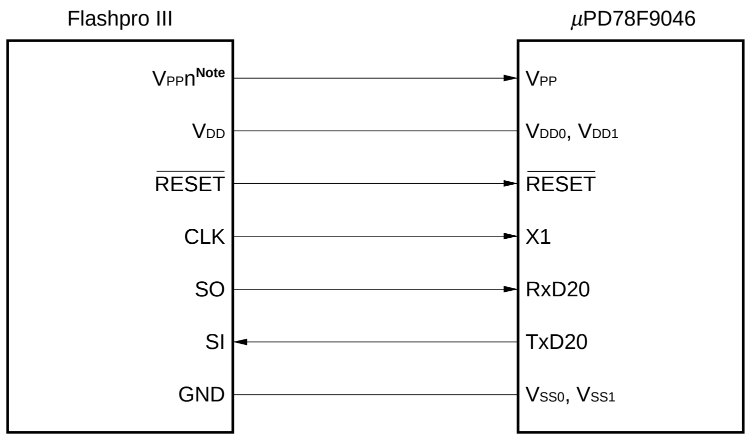
The connection of the Flashpro III and the μPD78F9046 differs according to the communication mode (3-wire serial I/O, UART, and pseudo 3-wire). The connections for each communication mode are shown in Figures 5-2, 5-3, and 5-4, respectively.

Figure 5-2. Connection of Flashpro III When Using 3-Wire Serial I/O Mode



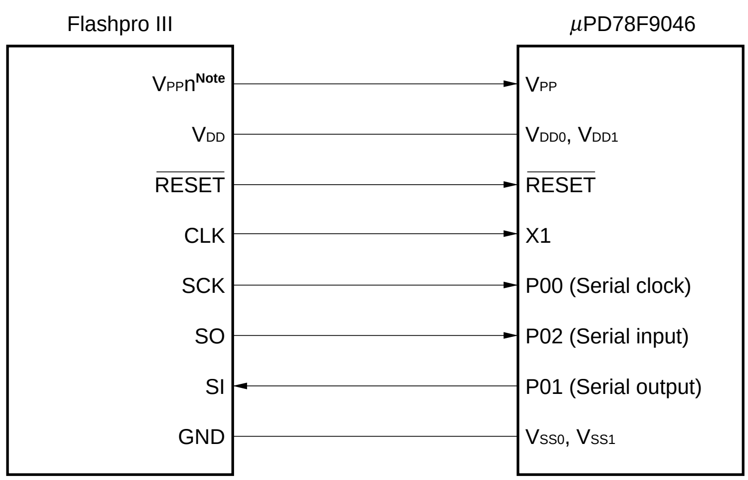
Note n = 0, 1

Figure 5-3. Connection of Flashpro III When Using UART Mode



Note n = 0, 1

Figure 5-4. Connection of Flashpro III When Using Pseudo 3-Wire (When P0 Is Used)



Note n = 0, 1

★ 5.4 Example of Settings for Flashpro III (PG-FP3)

When writing to flash memory using Flashpro III (PG-FP3), make the following settings.

<1> Load a parameter file.
<2> Select the mode of serial communication and serial clock with a type command.
<3> Make the settings according to the example of settings for PG-FP3 shown below.

Table 5-3. Example of Settings for PG-FP3

Communication Mode	Example of Settings for PG-FP3		V_{PP} Pulse Number[Note 1]
3-wire serial I/O	COMM PORT	SIO-ch0	0
	CPU CLK	On Target Board	
		In Flashpro	
	On Target Board	4.1943 MHz	
	SIO CLK	1.0 MHz	
	In Flashpro	4.0 MHz	
	SIO CLK	1.0 MHz	
UART	COMM PORT	UART-ch0	8
	CPU CLK	On Target Board	
	On Target Board	4.1943 MHz	
	UART BPS	9600 bps[Note 2]	
Pseudo 3-wire	COMM PORT	Port A	12
	CPU CLK	On Target Board	
		In Flashpro	
	On Target Board	4.1943 MHz	
	SIO CLK	1 kHz	
	In Flashpro	4.0 MHz	
	SIO CLK	1 kHz	

Notes **1.** This is the number of V_{PP} pulses that are supplied by the Flashpro III at serial communication initialization. The pins that will be used for communication are determined according to this number.

2. Select one of 9600 bps, 19200 bps, 38400 bps, or 76800 bps.

Remark COMM PORT: Serial port selection
SIO CLK: Serial clock frequency selection
CPU CLK: Input CPU clock source selection

6. INSTRUCTION SET OVERVIEW

The instruction set for the μPD78F9046 is listed later in this section.

6.1 Conventions

6.1.1 Operand identifiers and descriptions

The description made in the operand field of each instruction conforms to the operand identifier for the instructions listed below (the details conform to the assembly specifications). If more than one operand identifier is listed for an instruction, one is selected. Uppercase letters, #, !, $, and [ ] are used to specify keywords, which must be written exactly as they appear. The meanings of these special characters are as follows:

- #: Immediate data specification
- $: Relative address specification
- !: Absolute address specification
- [ ]: Indirect address specification

Immediate data should be described using appropriate values or labels. The specification of values and labels must be accompanied by #, !, $, or [ ].

Operand registers, expressed by the identifiers r or rp, can be described using both functional names (X, A, C, etc.) and absolute names (R0, R1, R2, and other names listed inside the parentheses in Table 6-1).

Table 6-1. Operand Formats and Descriptions

Identifier	Description
r rp sfr	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7) AX (RP0), BC (RP1), DE (RP2), HL (RP3) Special function register symbol
saddr saddrp	FE20H to FF1FH: Immediate data or label FE20H to FF1FH: Immediate data or label (even addresses only)
addr16 addr5	0000H to FFFFH: Immediate data or label (only even address for 16-bit data transfer instructions) 0040H to 007FH: Immediate data or label (even addresses only)
word byte bit	16-bit immediate data or label 8-bit immediate data or label 3-bit immediate data or label

6.1.2 Descriptions of the operation field

A: A register (8-bit accumulator)
X: X register
B: B register
C: C register
D: D register
E: E register
H: H register
L: L register
AX: AX register pair (16-bit accumulator)
BC: BC register pair
DE: DE register pair
HL: HL register pair
PC: Program counter
SP: Stack pointer
PSW: Program status word
CY: Carry flag
AC: Auxiliary carry flag
Z: Zero flag
IE: Interrupt request enable flag
NMIS: Flag to indicate that a non-maskable interrupt is being handled
(): Contents of a memory location indicated by a parenthesized address or register name
X_H, X_L: Upper and lower 8 bits of a 16-bit register
$\wedge$: Logical product (AND)
$\vee$: Logical sum (OR)
$\veebar$: Exclusive OR
$\overline{}$: Inverted data
addr16: 16-bit immediate data or label
jdisp8: Signed 8-bit data (displacement value)

6.1.3 Description of the flag operation field

(blank): No change
0: To be cleared to 0
1: To be set to 1
×: To be set or cleared according to the result
R: To be restored to the previous value

6.2 Operations

Mnemonic	Operand	Byte	Clock	Operation	Flag Z	Flag AC	Flag CY
MOV	r, #byte	3	6	r ← byte			
	saddr, #byte	3	6	(saddr) ← byte			
	sfr, #byte	3	6	sfr ← byte			
	A, r Note 1	2	4	A ← r			
	r, A Note 1	2	4	r ← A			
	A, saddr	2	4	A ← (saddr)			
	saddr, A	2	4	(saddr) ← A			
	A, sfr	2	4	A ← sfr			
	sfr, A	2	4	sfr ← A			
	A, !addr16	3	8	A ← (addr16)			
	!addr16, A	3	8	(addr16) ← A			
	PSW, #byte	3	6	PSW ← byte	×	×	×
	A, PSW	2	4	A ← PSW			
	PSW, A	2	4	PSW ← A	×	×	×
	A, [DE]	1	6	A ← (DE)			
	[DE], A	1	6	(DE) ← A			
	A, [HL]	1	6	A ← (HL)			
	[HL], A	1	6	(HL) ← A			
	A, [HL + byte]	2	6	A ← (HL + byte)			
	[HL + byte], A	2	6	(HL + byte) ← A			
XCH	A, X	1	4	A ↔ X			
	A, r Note 2	2	6	A ↔ r			
	A, saddr	2	6	A ↔ (saddr)			
	A, sfr	2	6	A ↔ (sfr)			
	A, [DE]	1	8	A ↔ (DE)			
	A, [HL]	1	8	A ↔ (HL)			
	A, [HL + byte]	2	8	A ↔ (HL + byte)			
MOVW	rp, #word	3	6	rp ← word			
	AX, saddrp	2	6	AX ← (saddrp)			
	saddrp, AX	2	8	(saddrp) ← AX			
	AX, rp Note 3	1	4	AX ← rp			
	rp, AX Note 3	1	4	rp ← AX			

Notes **1.** Except when r = A.

2. Except when r = A or X.

3. Only when rp = BC, DE, or HL.

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}), specified by the processor clock control register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
XCHW	AX, rp Note	1	8	AX ↔ rp			
ADD	A, #byte	2	4	A, CY ← A + byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte	×	×	×
	A, r	2	4	A, CY ← A + r	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A + (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte)	×	×	×
ADDC	A, #byte	2	4	A, CY ← A + byte + CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte + CY	×	×	×
	A, r	2	4	A, CY ← A + r + CY	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr) + CY	×	×	×
	A, !addr16	3	8	A, CY ← A + (addr16) + CY	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL) + CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte) + CY	×	×	×
SUB	A, #byte	2	4	A, CY ← A – byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte	×	×	×
	A, r	2	4	A, CY ← A – r	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte)	×	×	×
SUBC	A, #byte	2	4	A, CY ← A – byte – CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte – CY	×	×	×
	A, r	2	4	A, CY ← A – r – CY	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr) – CY	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16) – CY	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL) – CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte) – CY	×	×	×
AND	A, #byte	2	4	A ← A ∧ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∧ byte	×		
	A, r	2	4	A ← A ∧ r	×		
	A, saddr	2	4	A ← A ∧ (saddr)	×		
	A, !addr16	3	8	A ← A ∧ (addr16)	×		
	A, [HL]	1	6	A ← A ∧ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∧ (HL + byte)	×		

Note Only when rp = BC, DE, or HL.

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}), specified by the processor clock control register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag Z	Flag AC	Flag CY
OR	A, #byte	2	4	A ← A ∨ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∨ byte	×		
	A, r	2	4	A ← A ∨ r	×		
	A, saddr	2	4	A ← A ∨ (saddr)	×		
	A, !addr16	3	8	A ← A ∨ (addr16)	×		
	A, [HL]	1	6	A ← A ∨ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∨ (HL + byte)	×		
XOR	A, #byte	2	4	A ← A ⊻ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ⊻ byte	×		
	A, r	2	4	A ← A ⊻ r	×		
	A, saddr	2	4	A ← A ⊻ (saddr)	×		
	A, !addr16	3	8	A ← A ⊻ (addr16)	×		
	A, [HL]	1	6	A ← A ⊻ (HL)	×		
	A, [HL + byte]	2	6	A ← A ⊻ (HL + byte)	×		
CMP	A, #byte	2	4	A – byte	×	×	×
	saddr, #byte	3	6	(saddr) – byte	×	×	×
	A, r	2	4	A – r	×	×	×
	A, saddr	2	4	A – (saddr)	×	×	×
	A, !addr16	3	8	A – (addr16)	×	×	×
	A, [HL]	1	6	A – (HL)	×	×	×
	A, [HL + byte]	2	6	A – (HL + byte)	×	×	×
ADDW	AX, #word	3	6	AX, CY ← AX + word	×	×	×
SUBW	AX, #word	3	6	AX, CY ← AX – word	×	×	×
CMPW	AX, #word	3	6	AX – word	×	×	×
INC	r	2	4	r ← r + 1	×	×	
	saddr	2	4	(saddr) ← (saddr) + 1	×	×	
DEC	r	2	4	r ← r – 1	×	×	
	saddr	2	4	(saddr) ← (saddr) – 1	×	×	
INCW	rp	1	4	rp ← rp + 1			
DECW	rp	1	4	rp ← rp – 1			
ROR	A, 1	1	2	(CY, A_7 ← A_0, A_{m-1} ← A_m) × 1			×
ROL	A, 1	1	2	(CY, A_0 ← A_7, A_{m+1} ← A_m) × 1			×
RORC	A, 1	1	2	(CY ← A_0, A_7 ← CY, A_{m-1} ← A_m) × 1			×
ROLC	A, 1	1	2	(CY ← A_7, A_0 ← CY, A_{m+1} ← A_m) × 1			×

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}), specified by the processor clock control register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
SET1	saddr. bit	3	6	(saddr. bit) ← 1			
	sfr. bit	3	6	sfr. bit ← 1			
	A. bit	2	4	A. bit ← 1			
	PSW. bit	3	6	PSW. bit ← 1	×	×	×
	[HL]. bit	2	10	(HL). bit ← 1			
CLR1	saddr. bit	3	6	(saddr. bit) ← 0			
	sfr. bit	3	6	sfr. bit ← 0			
	A. bit	2	4	A. bit ← 0			
	PSW. bit	3	6	PSW. bit ← 0	×	×	×
	[HL]. bit	2	10	(HL). bit ← 0			
SET1	CY	1	2	CY ← 1			1
CLR1	CY	1	2	CY ← 0			0
NOT1	CY	1	2	CY ← $\overline{CY}$			×
CALL	!addr16	3	6	(SP – 1) ← $(PC + 3)_H$, (SP – 2) ← $(PC + 3)_L$, PC ← addr16, SP ← SP – 2			
CALLT	[addr5]	1	8	(SP – 1) ← $(PC + 1)_H$, (SP – 2) ← $(PC + 1)_L$, PC_H ← (00000000, addr5 + 1), PC_L ← (00000000, addr5), SP ← SP – 2			
RET		1	6	PC_H ← (SP + 1), PC_L ← (SP), SP ← SP + 2			
RETI		1	8	PC_H ← (SP + 1), PC_L ← (SP), PSW ← (SP + 2), SP ← SP + 3, NMIS ← 0	R	R	R
PUSH	PSW	1	2	(SP – 1) ← PSW, SP ← SP – 1			
	rp	1	4	(SP – 1) ← rp_H, (SP – 2) ← rp_L, SP ← SP – 2			
POP	PSW	1	4	PSW ← (SP), SP ← SP + 1	R	R	R
	rp	1	6	rp_H ← (SP + 1), rp_L ← (SP), SP ← SP + 2			
MOVW	SP, AX	2	8	SP ← AX			
	AX, SP	2	6	AX ← SP			
BR	!addr16	3	6	PC ← addr16			
	$addr16	2	6	PC ← PC + 2 + jdisp8			
	AX	1	6	PC_H ← A, PC_L ← X			

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}), specified by the processor clock control register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
BC	$addr16	2	6	PC ← PC + 2 + jdisp8 if CY = 1			
BNC	$addr16	2	6	PC ← PC + 2 + jdisp8 if CY = 0			
BZ	$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 1			
BNZ	$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 0			
BT	saddr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if (saddr. bit) = 1			
	sfr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr. bit = 1			
	A. bit, $addr16	3	8	PC ← PC + 3 + jdisp8 if A. bit = 1			
	PSW. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if PSW. bit = 1			
BF	saddr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if (saddr. bit) = 0			
	sfr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr. bit = 0			
	A. bit, $addr16	3	8	PC ← PC + 3 + jdisp8 if A. bit = 0			
	PSW. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if PSW. bit = 0			
DBNZ	B, $addr16	2	6	B ← B – 1, then PC ← PC + 2 + jdisp8 if B ≠ 0			
	C, $addr16	2	6	C ← C – 1, then PC ← PC + 2 + jdisp8 if C ≠ 0			
	saddr, $addr16	3	8	(saddr) ← (saddr) – 1, then PC ← PC + 3 + jdisp8 if (saddr) ≠ 0			
NOP		1	2	No Operation			
EI		3	6	IE ← 1 (Enable Interrupt)			
DI		3	6	IE ← 0 (Disable Interrupt)			
HALT		1	2	Set HALT Mode			
STOP		1	2	Set STOP Mode			

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}), specified by the processor clock control register (PCC).

7. ELECTRICAL SPECIFICATIONS

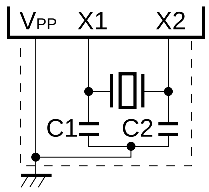
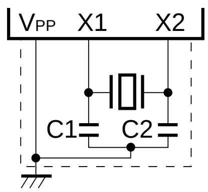
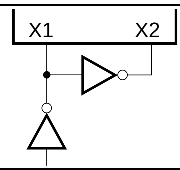
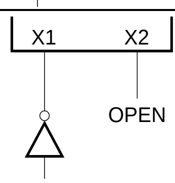
Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		–0.3 to +6.5	V
	V_{PP}		–0.3 to +10.5	V
Input voltage	V_I		–0.3 to V_{DD} + 0.3	V
Output voltage	V_O		–0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH}	Per pin	–10	mA
		Total for all pins	–30	mA
Output current, low	I_{OL}	Per pin	30	mA
		Total for all pins	160	mA
Operating ambient temperature	T_A	In normal operation mode	–40 to +85	°C
★		During flash memory programming	10 to 40	°C
Storage temperature	T_{stg}		–40 to +125	°C

Caution **Product quality may suffer if the maximum absolute ratings exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Main System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)Note 1	V_{DD} = Oscillation voltage range	1.0		5.0	MHz
		Oscillation stabilization timeNote 2	After V_{DD} reaches the oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequency (f_X)Note 1		1.0		5.0	MHz
		Oscillation stabilization timeNote 2	V_{DD} = 4.5 to 5.5 V			10	ms
						30	ms
External clock		X1 input frequency (f_X)Note 1		1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})		85		500	ns
★		X1 input frequency (f_X)Note 1	V_{DD} = 2.7 to 5.5 V	1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})	V_{DD} = 2.7 to 5.5 V	85		500	ns

Notes 1. Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release. Use a resonator whose oscillation is stabilized within the oscillation stabilization wait time.

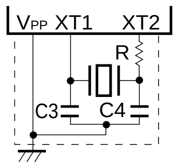
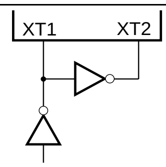
Cautions 1. When using the system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS0}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Subsystem Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})[Note 1]		32	32.768	35	kHz
		Oscillation stabilization time[Note 2]	V_{DD} = 4.5 to 5.5 V		1.2	2	s
						10	s
External clock		XT1 input frequency (f_{XT})[Note 1]		32		35	kHz
		X1 input high-/low-level width (t_{XTH}, t_{XTL})		14.3		15.6	μs

Notes 1. Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release. Use a resonator whose oscillation is stabilized within the oscillation stabilization wait time.

Cautions 1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuation current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as VSS0.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subsystem clock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

★ **DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high	I_{OH}	Per pin				–1	mA
		Total for all pins				–15	mA
Output current, low	I_{OL}	Per pin				10	mA
		Total for all pins				80	mA
Input voltage, high	V_{IH1}	P00 to P07, P10 to P17, P30, P31	V_{DD} = 2.7 to 5.5 V	$0.7V_{DD}$		V_{DD}	V
				$0.9V_{DD}$		V_{DD}	V
	V_{IH2}	$\overline{RESET}$, P20 to P27, P40 to P47,	V_{DD} = 2.7 to 5.5 V	$0.8V_{DD}$		V_{DD}	V
				$0.9V_{DD}$		V_{DD}	V
	V_{IH3}	X1, X2	V_{DD} = 4.5 to 5.5 V	V_{DD} – 0.5		V_{DD}	V
				V_{DD} – 0.1		V_{DD}	V
	V_{IH4}	XT1, XT2	V_{DD} = 4.5 to 5.5 V	V_{DD} – 0.5		V_{DD}	V
				V_{DD} – 0.1		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P07, P10 to P17, P30, P31	V_{DD} = 2.7 to 5.5 V	0		$0.3V_{DD}$	V
				0		$0.1V_{DD}$	V
	V_{IL2}	$\overline{RESET}$, P20 to P27, P40 to P47	V_{DD} = 2.7 to 5.5 V	0		$0.2V_{DD}$	V
				0		$0.1V_{DD}$	V
	V_{IL3}	X1, X2	V_{DD} = 4.5 to 5.5 V	0		0.4	V
				0		0.1	V
	V_{IL4}	XT1, XT2	V_{DD} = 4.5 to 5.5 V	0		0.4	V
				0		0.1	V
Output voltage, high	V_{OH}	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1 mA		V_{DD} – 1.0			V
		V_{DD} = 1.8 to 5.5 V, I_{OH} = –100 μA		V_{DD} – 0.5			V
Output voltage, low	V_{OL}	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA				1.0	V
		V_{DD} = 1.8 to 5.5 V, I_{OL} = 400 μA				0.5	V
Input leakage current, high	I_{LIH1}	$V_{IN} = V_{DD}$	Pins other than X1, X2, XT1, XT2			3	μA
	I_{LIH2}		X1, X2			20	μA
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	Pins other than X1, X2, XT1, XT2			–3	μA
	I_{LIL2}		X1, X2			–20	μA
Output leakage current, high	I_{LOH}	$V_{OUT} = V_{DD}$				3	μA
Output leakage current, low	I_{LOL}	V_{OUT} = 0 V				–3	μA
Software pull-up resistor	R	V_{IN} = 0 V		50	100	200	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

★ **DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD1}	5.0-MHz crystal oscillation operating mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ± 10%[Note 3]		4.2	15	mA
			V_{DD} = 3.0 V ± 10%[Note 4]		1.0	5.0	mA
			V_{DD} = 2.0 V ± 10%[Note 4]		0.8	3.0	mA
	I_{DD2}	5.0-MHz crystal oscillation HALT mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ± 10%[Note 3]		0.8	5.0	mA
			V_{DD} = 3.0 V ± 10%[Note 4]		0.5	2.5	mA
			V_{DD} = 2.0 V ± 10%[Note 4]		0.3	1.0	mA
	I_{DD3}	32.768-kHz crystal oscillation operating mode[Note 2] (C3 = C4 = 22 pF, R = 220 kΩ)	V_{DD} = 5.0 V ± 10%		200	750	μA
			V_{DD} = 3.0 V ± 10%		150	600	μA
			V_{DD} = 2.0 V ± 10%		130	450	μA
	I_{DD4}	32.768-kHz crystal oscillation HALT mode[Note 2] (C3 = C4 = 22 pF, R = 220 kΩ)	V_{DD} = 5.0 V ± 10%		25	150	μA
			V_{DD} = 3.0 V ± 10%		10	90	μA
			V_{DD} = 2.0 V ± 10%		3.5	60	μA
	I_{DD5}	STOP mode	V_{DD} = 5.0 V ± 10%		0.1	30	μA
			V_{DD} = 3.0 V ± 10%		0.05	10	μA
			V_{DD} = 2.0 V ± 10%		0.05	10	μA

Notes 1. The current flowing to the ports (including the current flowing through the on-chip pull-up resistors) is not included.

2. Main system clock stopped.

3. High-speed mode operation (when the processor clock control register (PCC) is set to 00H).

4. Low-speed mode operation (when PCC is set to 02H).

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

★ **Flash Memory Write/Erase Characteristics**

(T_A = 10 to 40°C, V_{DD} = 1.8 to 5.5 V, in 5.0 MHz crystal oscillation operation mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Write current[Note] (V_{DD} pin)	I_{DDW}	When V_{PP} supply voltage = V_{PP1}			18	mA
Write current[Note] (V_{PP} pin)	I_{PPW}	When V_{PP} supply voltage = V_{PP1}			22.5	mA
Erase current[Note] (V_{DD} pin)	I_{DDE}	When V_{PP} supply voltage = V_{PP1}			18	mA
Erase current[Note] (V_{PP} pin)	I_{PPE}	When V_{PP} supply voltage = V_{PP1}			115	mA
Unit erase time	t_{er}		0.5	1	1	s
Total erase time	t_{era}				20	s
Write count		Erase/write are regarded as 1 cycle			20	Times
V_{PP} supply voltage	V_{PP0}	In normal operation	0		$0.2V_{DD}$	V
	V_{PP1}	During flash memory programming	9.7	10.0	10.3	V

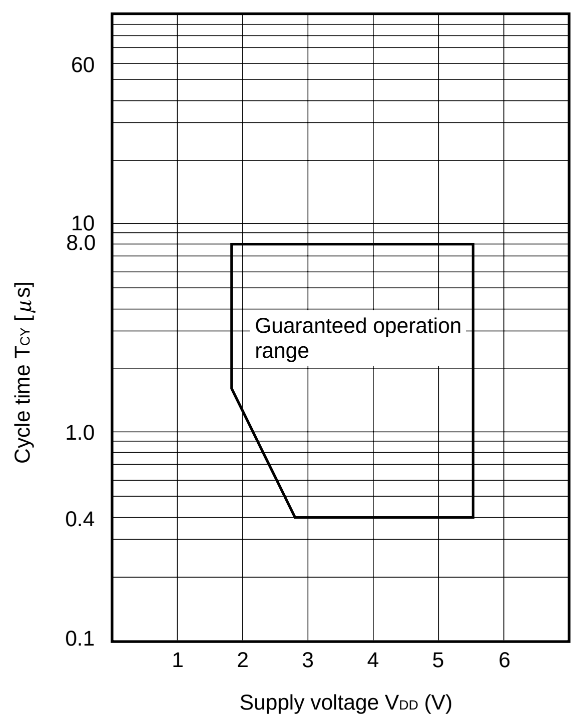
Note The current flowing to the ports (including the current flowing through the on-chip pull-up resistors) is not included.

AC Characteristics

(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	Operating with main system clock	V_{DD} = 2.7 to 5.5 V	0.4		8	μs
				1.6		8	μs
		Operating with subsystem clock		114	122	125	μs
TI80 input frequency	f_{TI}	V_{DD} = 2.7 to 5.5 V		0		4	MHz
				0		275	kHz
TI80 input high-/low-level width	t_{TIH}, t_{TIL}	V_{DD} = 2.7 to 5.5 V		0.1			μs
				1.8			μs
★ Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP2		10			μs
★ $\overline{\text{RESET}}$ input low-level width	t_{RSL}			10			μs

T_{CY} vs. V_{DD} (main system clock)



(2) Serial interface (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

(a) 3-wire serial I/O mode (SCK20...Internal clock)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCK20 cycle time	t_{KCY1}	V_{DD} = 2.7 to 5.5 V	800			ns
			3200			ns
SCK20 high-/low-level width	t_{KH1}, t_{KL1}	V_{DD} = 2.7 to 5.5 V	t_{KCY1}/2 – 50			ns
			t_{KCY1}/2 – 150			ns
SI20 setup time (to SCK20↑)	t_{SIK1}	V_{DD} = 2.7 to 5.5 V	150			ns
			500			ns
SI20 hold time (from SCK20↑)	t_{KSI1}	V_{DD} = 2.7 to 5.5 V	400			ns
			600			ns
SO20 output delay time from SCK20↓	t_{KSO1}	R = 1 kΩ, C =100 pF[Note], V_{DD} = 2.7 to 5.5 V	0		250	ns
			0		1000	ns

Note R and C are the load resistance and load capacitance of the SO20 output line, respectively.

(b) 3-wire serial I/O mode (SCK20...External clock)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
★ SCK20 cycle time	t_{KCY2}	V_{DD} = 2.7 to 5.5 V	900			ns
			3500			ns
SCK20 high-/low-level width	t_{KH2}, t_{KL2}	V_{DD} = 2.7 to 5.5 V	400			ns
			1600			ns
SI20 setup time (to SCK20↑)	t_{SIK2}	V_{DD} = 2.7 to 5.5 V	100			ns
			150			ns
SI20 hold time (from SCK20↑)	t_{KSI2}	V_{DD} = 2.7 to 5.5 V	400			ns
			600			ns
★ SO20 setup time (to SS20↓ when SS20 is used)	t_{KAS2}	V_{DD} = 2.7 to 5.5 V			120	ns
					400	ns
★ SO20 disable time (to SS20↑ when SS20 is used)	t_{KSD2}	V_{DD} = 2.7 to 5.5 V			240	ns
					800	ns
SO20 output delay time from SCK20↓	t_{KSO2}	R = 1 kΩ, C =100 pF[Note], V_{DD} = 2.7 to 5.5 V	0		300	ns
			0		1000	ns

Note R and C are the load resistance and load capacitance of the SO20 output line, respectively.

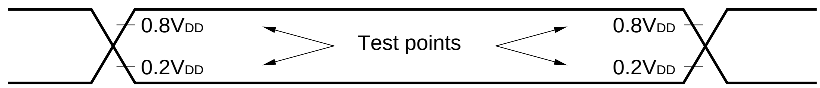
(c) UART mode (Dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		V_{DD} = 2.7 to 5.5 V			78125	bps
					19531	bps

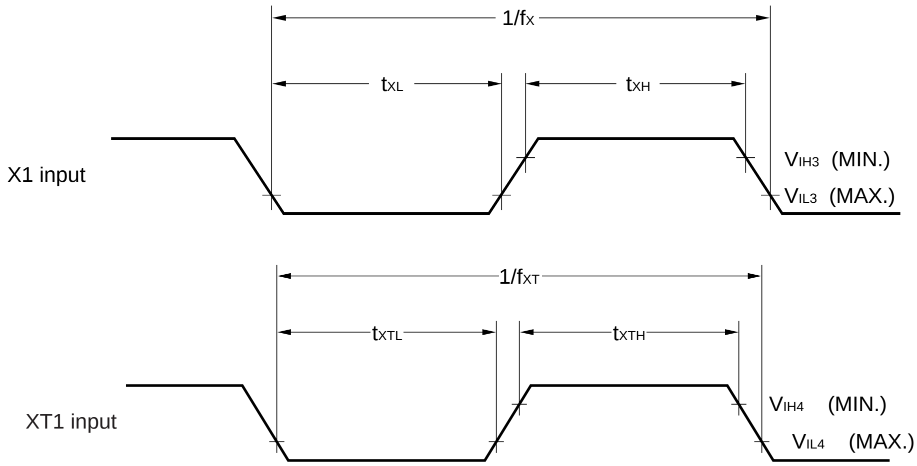
(d) UART mode (External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
★ ASCK20 cycle time	t_{KCY3}	V_{DD} = 2.7 to 5.5 V	900			ns
			3500			ns
ASCK20 high-/low-level width	t_{KH3}, t_{KL3}	V_{DD} = 2.7 to 5.5 V	400			ns
			1600			ns
Transfer rate		V_{DD} = 2.7 to 5.5 V			39063	bps
					9766	bps
ASCK20 rise/fall time	t_R, t_F				1	μs

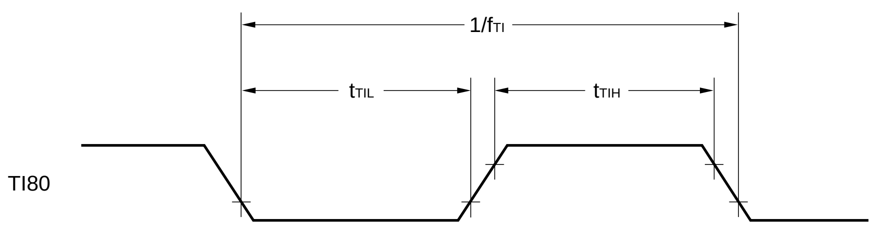
AC Timing Test Points (Except the X1 and XT1 inputs)



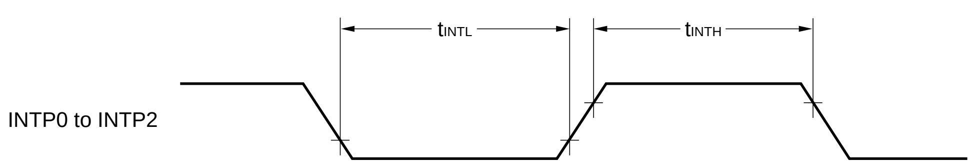
Clock Timing



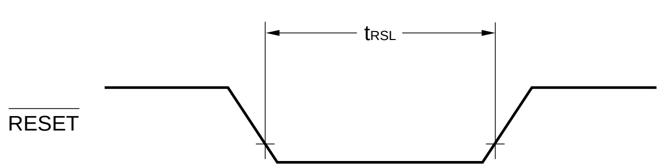
TI Timing



Interrupt Input Timing

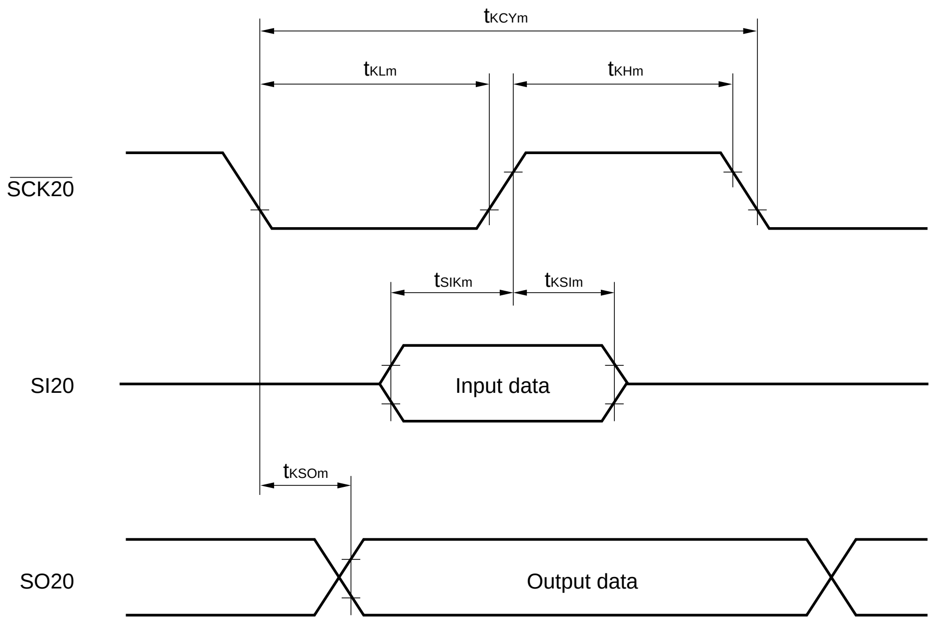


$\overline{\text{RESET}}$ Input Timing



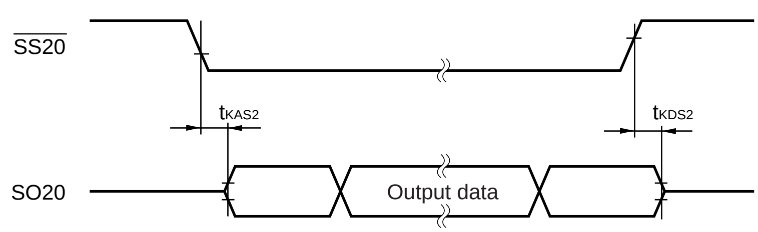
Serial Transfer Timing

3-wire serial I/O mode:

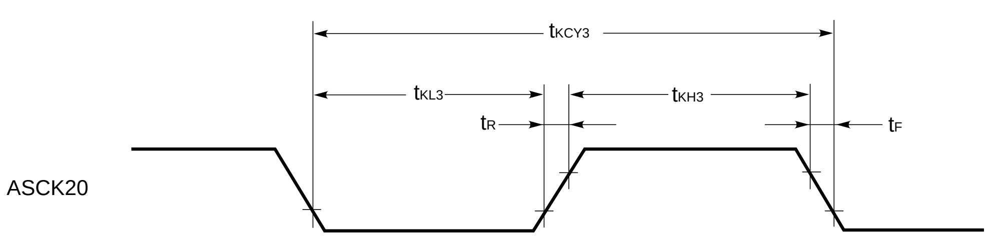


Remark m = 1, 2

3-wire serial I/O mode (when $\overline{SS20}$ is used):



UART mode (External clock input):



Data Memory Stop Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

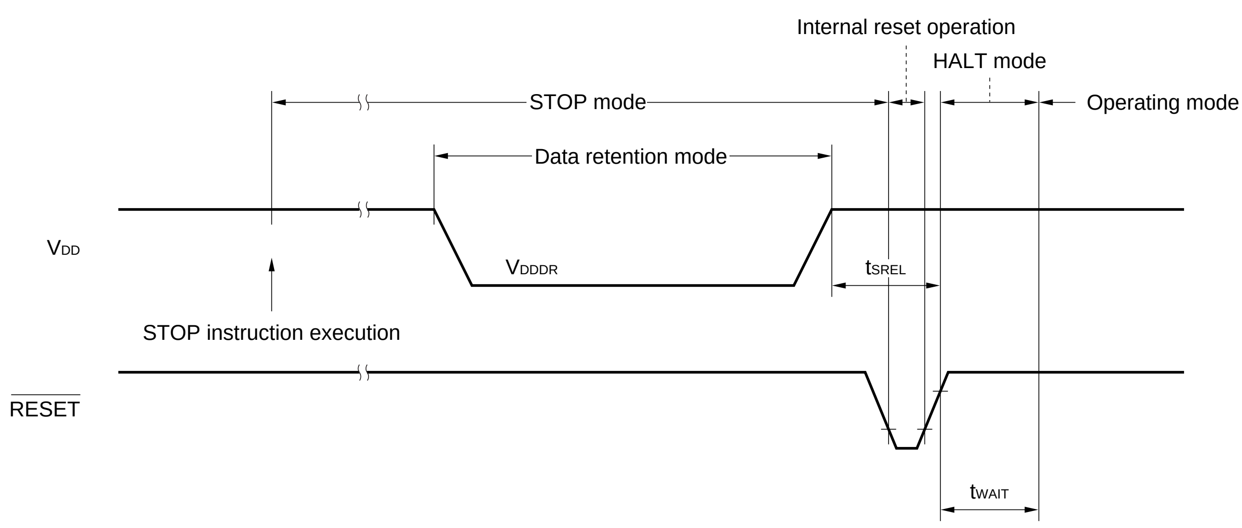
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.8		5.5	V
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time[Note 1]	t_{WAIT}	Release by $\overline{RESET}$		$2^{15}/f_X$		ms
		Release by interrupt request		**Note 2**		ms

Notes 1. The oscillation stabilization wait time is the period when CPU operation is stopped in order to avoid unstable operation at the beginning of oscillation.

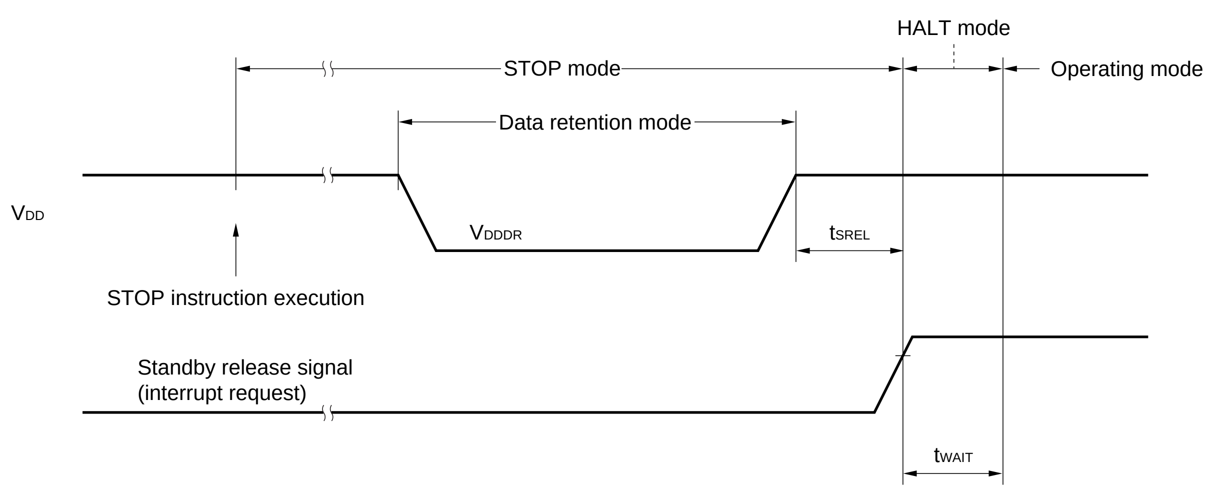
2. $2^{12}/f_X$, $2^{15}/f_X$, or $2^{17}/f_X$ can be selected according to the setting of bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time selection register (OSTS).

Remark f_X: Main system clock oscillation frequency

Data Retention Timing (STOP Mode Release by $\overline{RESET}$)

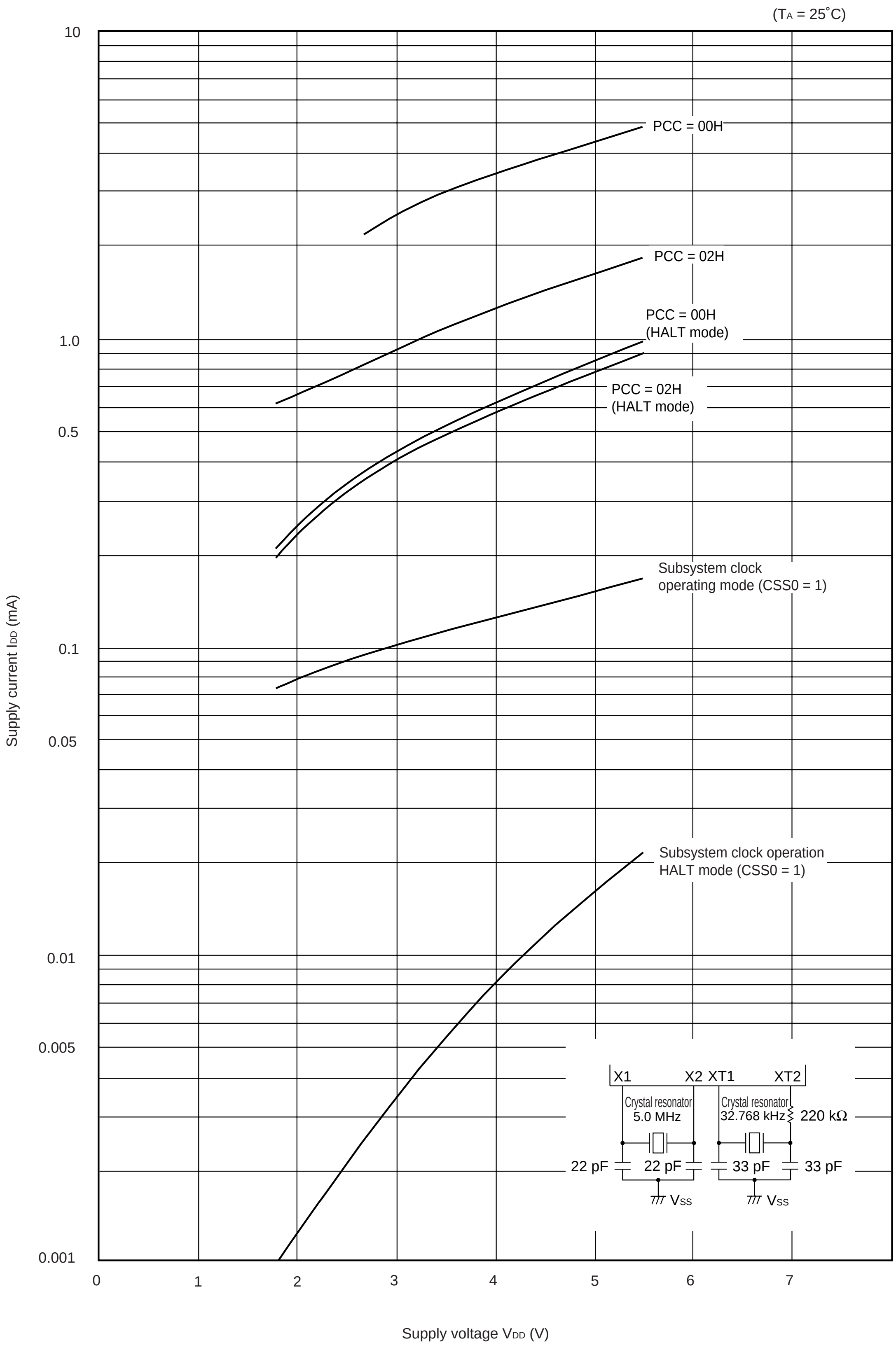


★ **Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)**



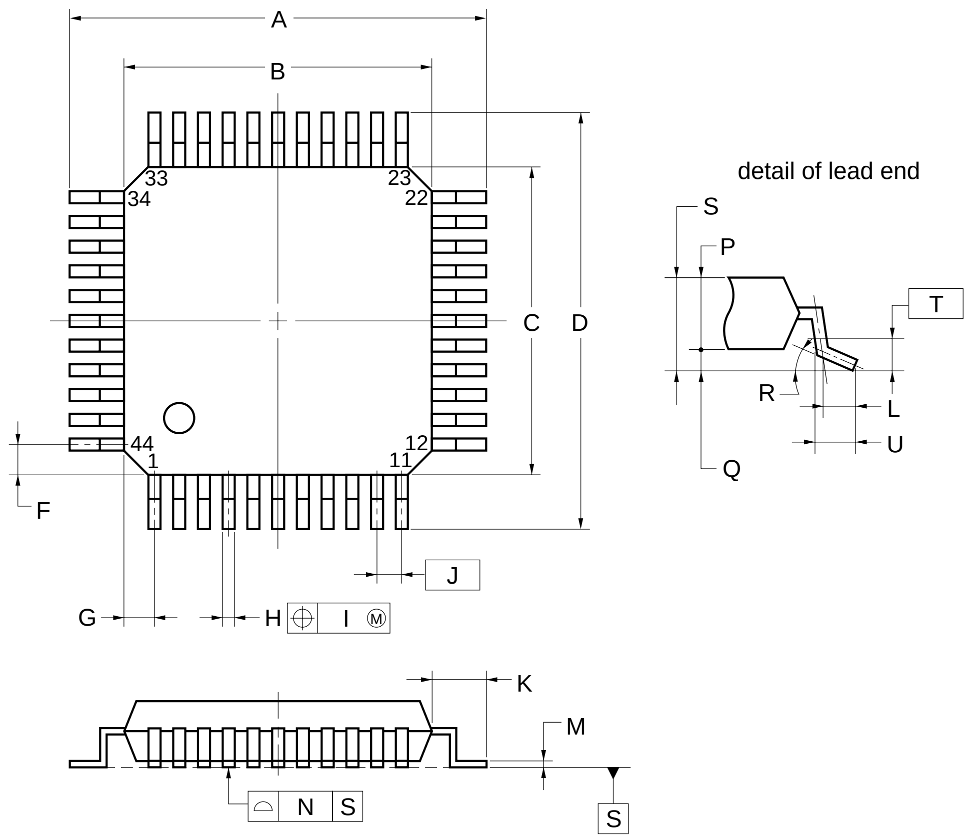
★ 8. CHARACTERISTICS CURVES

IDD vs. VDD (fX = 5.0 MHz, fXT = 32.768 kHz)



9. PACKAGE DRAWINGS

44 PIN PLASTIC LQFP (10x10)



NOTE

Each lead centerline is located within 0.16 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	12.0±0.2
B	10.0±0.2
C	10.0±0.2
D	12.0±0.2
F	1.0
G	1.0
H	$0.37^{+0.08}_{-0.07}$
I	0.2
J	0.8 (T.P.)
K	1.0±0.2
L	0.5
M	$0.17^{+0.03}_{-0.06}$
N	0.10
P	1.4±0.05
Q	0.1±0.05
R	$3°^{+4°}_{-3°}$
S	1.6 MAX.
U	0.6±0.15

S44GB-80-8ES-1

★ 10. RECOMMENDED SOLDERING CONDITIONS

The μPD78F9046 should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Table 10-1. Surface Mounting Type Soldering Conditions

μPD78F9046GB-8ES: 44-pin plastic LQFP (10 × 10 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: twice or less	IR35-00-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: twice or less	VP15-00-2
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once, Preheating temperature: 120°C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	—

Caution Do not use different soldering methods together (except for partial heating).

APPENDIX A DIFFERENCES BETWEEN μPD78F9046 AND MASK ROM VERSIONS

The μPD78F9046 has flash memory in place of the internal ROM of the mask ROM versions (μPD789046). Differences between the μPD78F9046 and mask ROM versions are shown in Table A-1.

Table A-1. Differences Between μPD78F9046A and Mask ROM Versions

Parameter		Flash Memory Version	Mask ROM Versions
		μPD78F9046	μPD789046
Internal memory	ROM structure	Flash memory	Mask ROM
	ROM capacity	16 Kbytes	
	High-speed RAM capacity	512 bytes	
V_{PP} pin		Available	Not available
IC pin		Not available	Available
Electrical specifications		See the relevant data sheet	

Caution There are differences in noise immunity and noise radiation between the flash memory and mask ROM versions. When pre-producing an application set with the flash memory version and then mass-producing it with the mask ROM version, be sure to conduct sufficient evaluations for the consumer samples (not engineering samples) of the mask ROM version.

APPENDIX B DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD78F9046.

Language Processing Software

RA78K0S[Notes 1, 2, 3]	Assembler package common to 78K/0S Series
CC78K0S[Notes 1, 2, 3]	C compiler package common to 78K/0S Series
DF789026[Notes 1, 2, 3]	Device file for the μPD789046 Subseries
★ CC78K0S-L[Notes 1, 2, 3]	C compiler library source file common to 78K/0S Series

★ Flash Memory Writing Tools

Flashpro lll (FL-PR3[Note 4], PG-FP3)	Dedicated flash programmer for microcontrollers incorporating flash memory
FA-44GB-8ES[Note 4]	Flash memory writing adapter for 44-pin plastic LQFP (GB-8ES type)

Debugging Tools

IE-78K0S-NS In-circuit emulator	In-circuit emulator for debugging the hardware and software of the application system using the 78K/0S series. Supports the integrated debugger (ID78K0S-NS). Used with an AC adapter, emulation probe, and interface adapter that connects the host machine.
IE-70000-MC-PS-B AC adapter	Adapter that distributes power supply from an AC100- to 240-V outlet.
IE-70000-98-IF-C Interface adapter	Adapter when using a PC-9800 series PC (except notebook type) as the host machine of the IE-78K0S-NS (C bus supported).
IE-70000-CD-IF-A PC card interface	PC card and interface cable when using a notebook type PC as the host machine of the IE-78K0S-NS (PCMCIA socket supported).
IE-70000-PC-IF-C Interface adapter	Adapter when using an IBM PC/AT™ or compatible as the host machine of the IE-78K0S-NS (ISA bus supported).
★ IE-70000-PCI-IF Interface adapter	Adapter when using a PC with PCI bus as the host machine of the IE-78K0S-NS.
IE-789026-NS-EM1 Emulation board	Board for emulating device-specific peripheral hardware. Used with an in-circuit emulator.
NP-44GB[Note 4] ★ NP-44GB-TQ[Note 4]	Board connecting an in-circuit emulator and target system. For 44-pin plastic LQFP (GB-3BS type) and 44-pin plastic LQFP (GB-8ES type).
SM78K0S[Notes 1,2]	System simulator common to 78K/0S Series
★ ID78K0S-NS[Notes 1,2]	Integrated debugger common to 78K/0S Series
DF789046[Notes 1,2]	Device file for μPD789046 Subseries

Real-Time OS

MX78K0S[Notes 1, 2]	OS for 78K/0S Series

Notes 1. Based on the PC-9800 series (Japanese/English Windows™)

2. Based on IBM PC/AT and compatibles (Japanese/English Windows)

3. Based on the HP9000 series 700™ (HP-UX™), SPARCstation™ (SunOS™, Solaris™), and NEWS™ (NEWS-OS™)

4. Products manufactured by Naito Densei Machida Mfg. Co., Ltd. (+81-44-822-3813). Contact an NEC distributor regarding the purchase of these products.

Remark The RA78K0S, CC78K0S, and SM78K0S can be used in combination with the DF789046.

APPENDIX C RELATED DOCUMENTS

★ Documents Related to Devices

Document Name	Document No. English	Document No. Japanese
μPD789046 Data Sheet	U13380E	U13380J
μPD78F9046 Data Sheet	This manual	U13546J
μPD789046 Subseries User's Manual	U13600E	U13600J
78K/0S Series User's Manual — Instruction	U11047E	U11047J
78K/0, 78K/0S Series Application Note — Flash Memory Write	U14458E	U14458J

Documents Related to Development Tools (User's Manuals)

Document Name		Document No. English	Document No. Japanese
RA78K0S Assembler Package	Operation	U11622E	U11622J
	Assembly Language	U11599E	U11599J
	Structured Assembly Language	U11623E	U11623J
CC78K0S C Compiler	Operation	U11816E	U11816J
	Language	U11817E	U11817J
SM78K0S System Simulator Windows Based	Reference	U11489E	U11489J
SM78K Series System Simulator	External Parts User Open Interface Specifications	U10092E	U10092J
ID78K0S-NS Integrated Debugger Windows Based	Reference	U12901E	U12901J
★ IE-78K0S-NS In-Circuit Emulator		U13549E	U13549J
★ IE-789046-NS-EM1 Emulation Board		To be prepared	To be prepared

Documents Related to Embedded Software (User's Manuals)

Document Name		Document No. English	Document No. Japanese
78K/0S Series OS MX78K0S	Fundamental	U12938E	U12938J

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

Other Related Documents

Document Name	Document No.	
	English	Japanese
★ SEMICONDUCTOR SELECTION GUIDE Products & Packages (CD-ROM)	X13769X	
Semiconductor Device Mounting Technology Manual	C10535E	C10535J
Quality Grades on NEC Semiconductor Device	C11531E	C11531J
NEC Semiconductor Device Reliability/Quality Control System	C10983E	C10983J
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E	C11892J
Guide to Microcomputer-Related Products by Third Party	—	U11416J

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[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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Solaris and SunOS are trademarks of Sun Microsystems, Inc.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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