NEC

MOS INTEGRATED CIRCUIT

μPD78F0034AY

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD78F0034AY is a product of the μPD780034AY Subseries in the 78K/0 Series, and is equivalent to the μPD780034AY but with flash memory in place of internal ROM.

The μPD78F0034AY incorporates flash memory, which can be programmed and erased while mounted on the board.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD780024A, 780034A, 780024AY, 780034AY Subseries User's Manual: U14046E
78K/0 Series User's Manual Instruction: U12326E

FEATURES

- On-chip I^2C bus serial interface supported multimaster
- Pin-compatible with mask ROM versions (except V_{PP} pin)
- Flash memory: 32 Kbytes**Note**
- Internal high-speed RAM: 1024 bytes**Note**
- Supply voltage: V_{DD} = 1.8 to 5.5 V

Note The flash memory and internal high-speed RAM capacities can be changed with the memory size switching register (IMS).

Remark For the differences between the flash memory and the mask ROM versions, refer to **1. DIFFERENCES BETWEEN μPD78F0034AY AND MASK ROM VERSIONS**.

ORDERING INFORMATION

Part Number	Package	Internal ROM
μPD78F0034AYCW	64-pin plastic shrink DIP (750 mils)	Flash memory
μPD78F0034AYGC-AB8	64-pin plastic QFP (14 × 14 mm)	Flash memory
μPD78F0034AYGK-8A8	64-pin plastic LQFP (12 × 12 mm)	Flash memory

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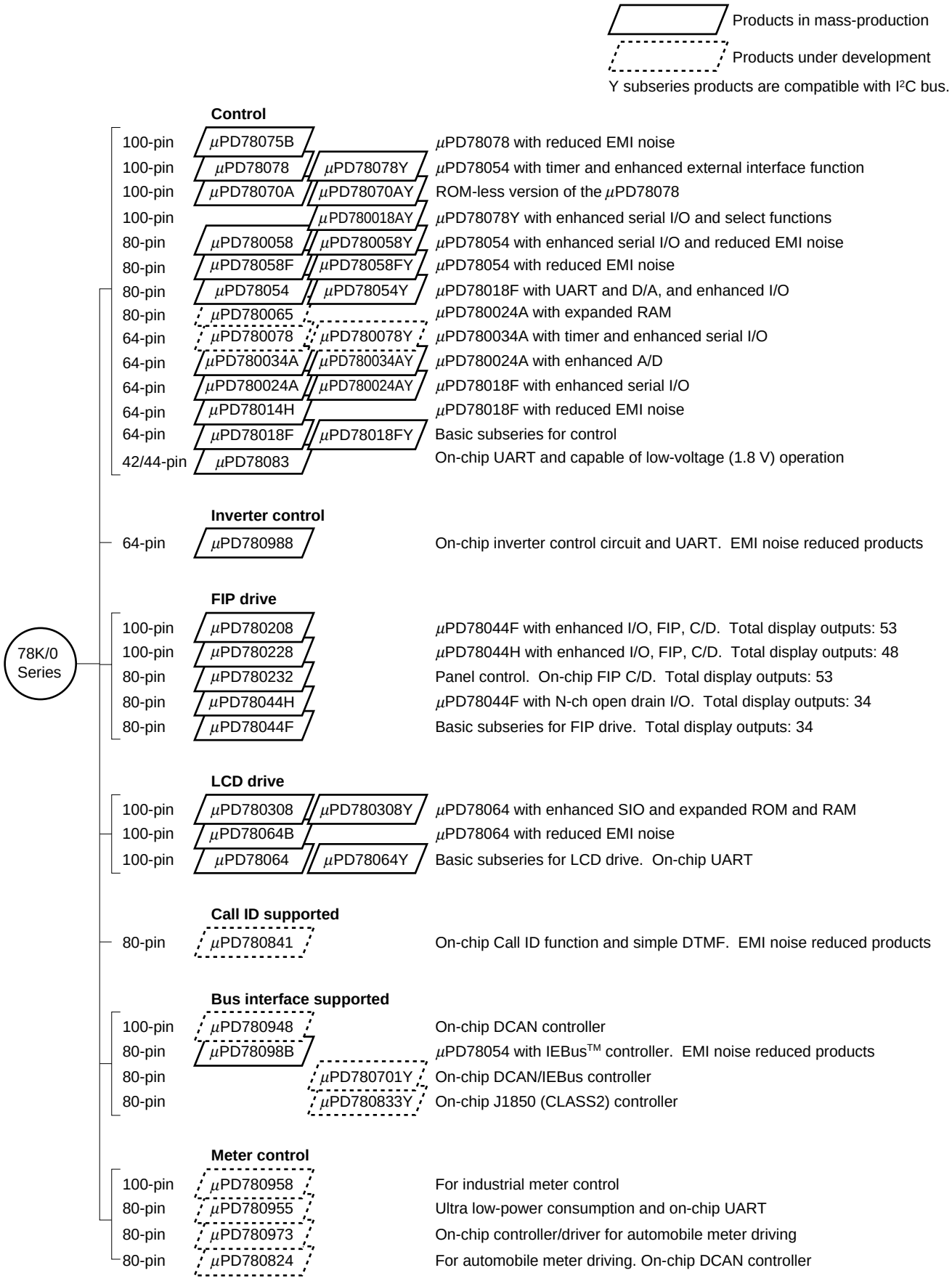
78K/0 SERIES LINEUP

The products in the 78K/0 Series are listed below. The names enclosed in boxes are subseries names.



The major functional differences among the Y subseries are shown below.

Subseries Name \ Function		ROM Capacity	Configuration of Serial Interface	I/O	V_{DD} MIN. Value
Control	μPD78078Y	48 K to 60 K	3-wire/2-wire/I^2C: 1 ch	88	1.8 V
	μPD78070AY	—	3-wire with automatic transmit/receive function: 1 ch 3-wire/UART: 1 ch	61	2.7 V
	μPD780018AY	48 K to 60 K	3-wire with automatic transmit/receive function: 1 ch Time-division 3-wire: 1 ch I^2C bus (multimaster supported): 1 ch	88	
	μPD780058Y	24 K to 60 K	3-wire/2-wire/I^2C: 1 ch 3-wire with automatic transmit/receive function: 1 ch 3-wire/time-division UART: 1 ch	68	1.8 V
	μPD78058FY	48 K to 60 K	3-wire/2-wire/I^2C: 1 ch	69	2.7 V
	μPD78054Y	16 K to 60 K	3-wire with automatic transmit/receive function: 1 ch 3-wire/UART: 1 ch		2.0 V
	μPD780078Y	48 K to 60 K	3-wire 1 ch UART: 1 ch 3-wire/UART: 1 ch I^2C bus (multimaster supported): 1 ch	52	1.8 V
	μPD780034AY	8 K to 32 K	UART: 1 ch 3-wire: 1 ch I^2C bus (multimaster supported): 1 ch	51	1.8 V
	μPD780024AY				
	μPD78018FY	8 K to 60 K	3-wire/2-wire/I^2C: 1 ch 3-wire with automatic transmit/receive function: 1 ch	53	
LCD drive	μPD780308Y	48 K to 60 K	3-wire/2-wire/I^2C: 1 ch 3-wire/time-division UART: 1 ch 3-wire: 1 ch	57	2.0 V
	μPD78064Y	16 K to 32 K	3-wire/2-wire/I^2C: 1 ch 3-wire/UART: 1 ch		

Remark Functions other than the serial interface are common to the non-Y subseries

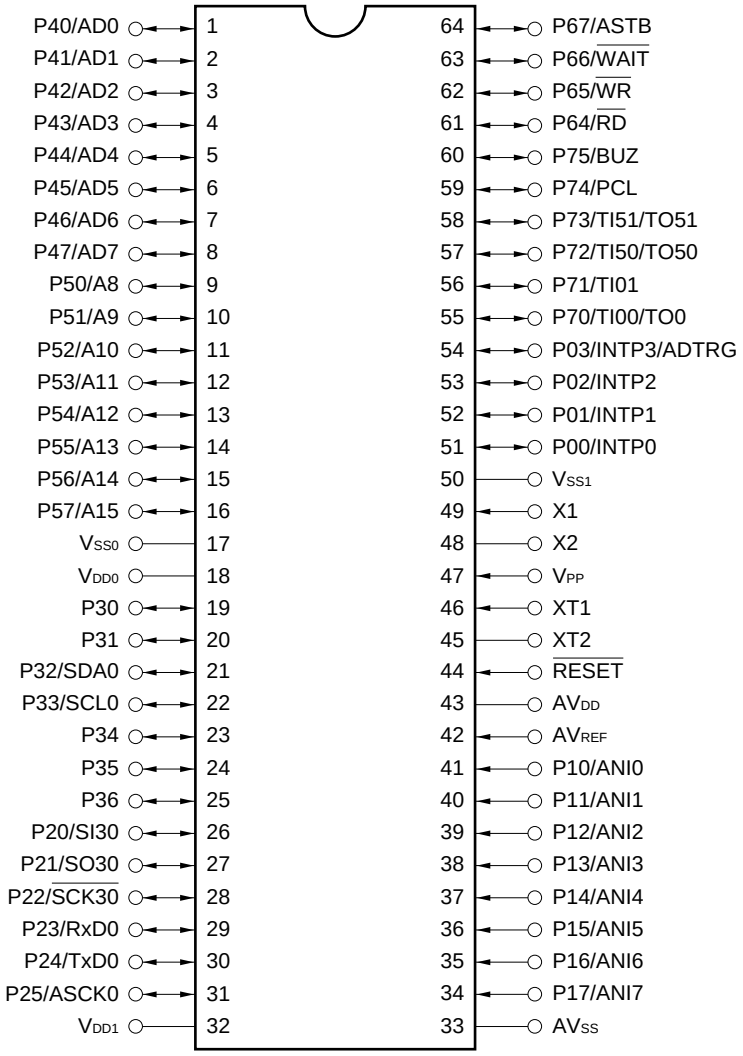
OVERVIEW OF FUNCTIONS

Item		Function
Internal memory	Flash memory	32 Kbytes[Note]
	High-speed RAM	1024 bytes[Note]
Memory space		64 Kbytes
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)
Minimum instruction execution time		On-chip minimum instruction execution time cycle modification function
	When main system clock selected	0.24 μs/0.48 μs/0.95 μs/1.91 μs/3.81 μs (@ 8.38-MHz operation)
	When subsystem clock selected	122 μs (@ 32.768-kHz operation)
Instruction set		• 16-bit operation, multiply/divide (8 bits × 8 bits,16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, Boolean operation) • BCD adjust, etc.
I/O ports		Total: 51 • CMOS input: 8 • CMOS I/O: 39 • N-ch open drain I/O (5-V resistance): 4
A/D converter		• 10-bit resolution × 8 channels • Operable over a wide power supply voltage range: AV_{DD} = 1.8 to 5.5 V
Serial interface		• 3-wire serial I/O mode: 1 channel • UART mode: 1 channel • I^2C bus mode (multimaster supported): 1 channel
Timer		• 16-bit timer/event counter: 1 channel • 8-bit timer/event counter: 2 channels • Watch timer: 1 channel • Watchdog timer: 1 channel
Timer outputs		3 (8-bit PWM output capable 2)
Clock output		65.5 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.10 MHz, 4.19 MHz, 8.38 MHz (@ 8.38-MHz operation with main system clock) 32.768 kHz (@ 32.768-kHz operation with subsystem clock)
Buzzer output		1.02 kHz, 2.05 kHz, 4.10 kHz, 8.19 kHz (@ 8.38-MHz operation with main system clock)
Vectored interrupt sources	Maskable	Internal: 13 External: 5
	Non-maskable	Internal: 1
	Software	1
Test inputs		Internal: 1 External: 1
Supply voltage		V_{DD} = 1.8 to 5.5 V
Operating ambient temperature		T_A = –40 to +85°C
Package		• 64-pin plastic shrink DIP (750 mils) • 64-pin plastic QFP (14 × 14 mm) • 64-pin plastic LQFP (12 × 12 mm)

Note The capacities of the flash memory and the internal high-speed RAM can be changed with the memory size switching register (IMS).

PIN CONFIGURATION (TOP VIEW)

- **64-pin plastic shrink DIP (750 mils)**
  μPD78F0034AYCW

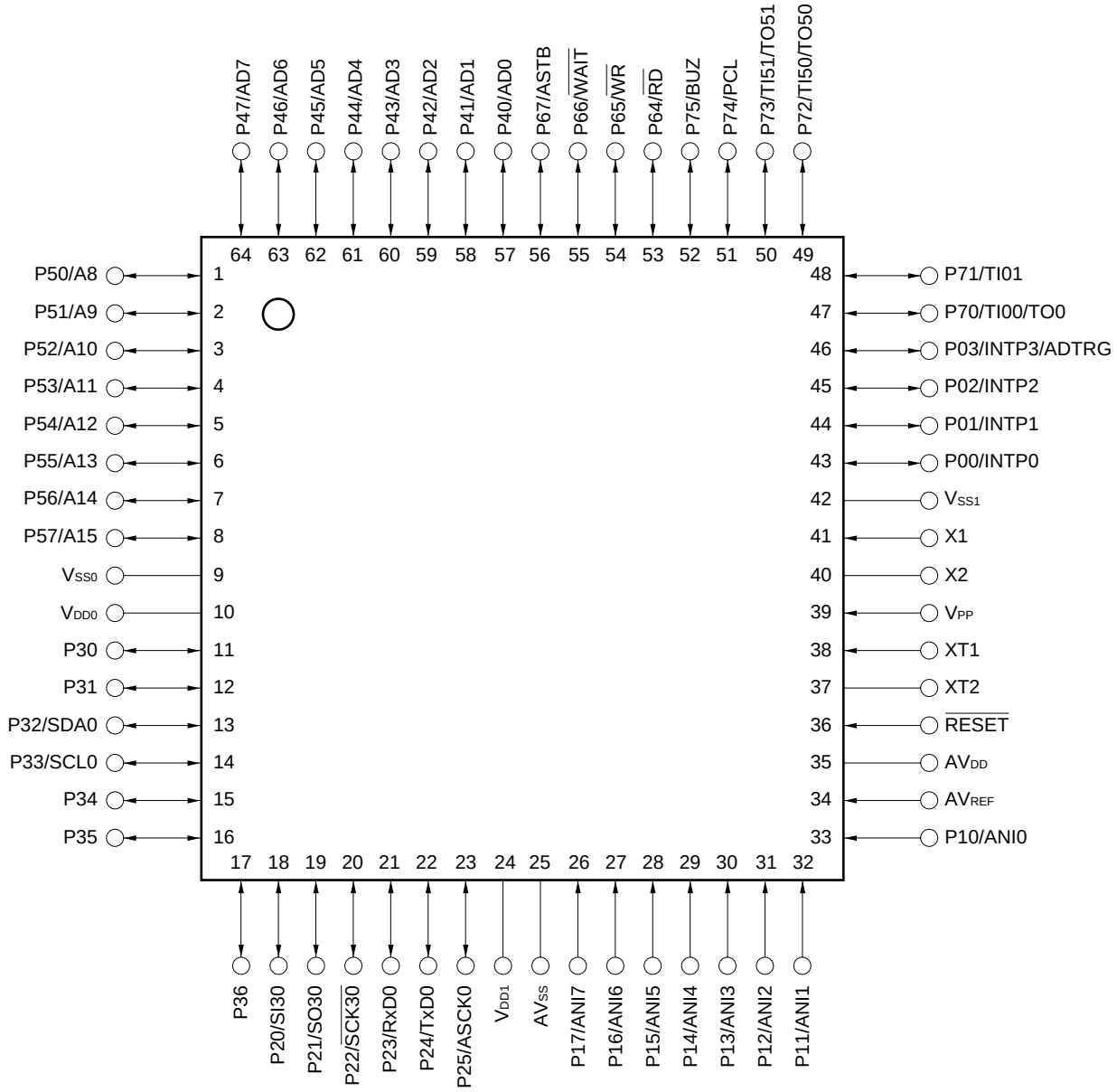


Cautions 1. Connect the V_{PP} pin directly to V_{SS0} or V_{SS1} in normal operation mode.

2. Connect the AV_{SS} pin to V_{SS0}.

Remark When the μPD78F0034AY is used in application fields that require reduction of the noise generated from inside the microcontroller, the implementation of noise reduction measures, such as supplying voltage to V_{DD0} and V_{DD1} individually and connecting V_{SS0} and V_{SS1} to different ground lines, is recommended.

- **64-pin plastic QFP (14 × 14 mm)**
  μPD78F0034AYGC-AB8
- **64-pin plastic LQFP (12 × 12 mm)**
  μPD78F0034AYGK-8A8



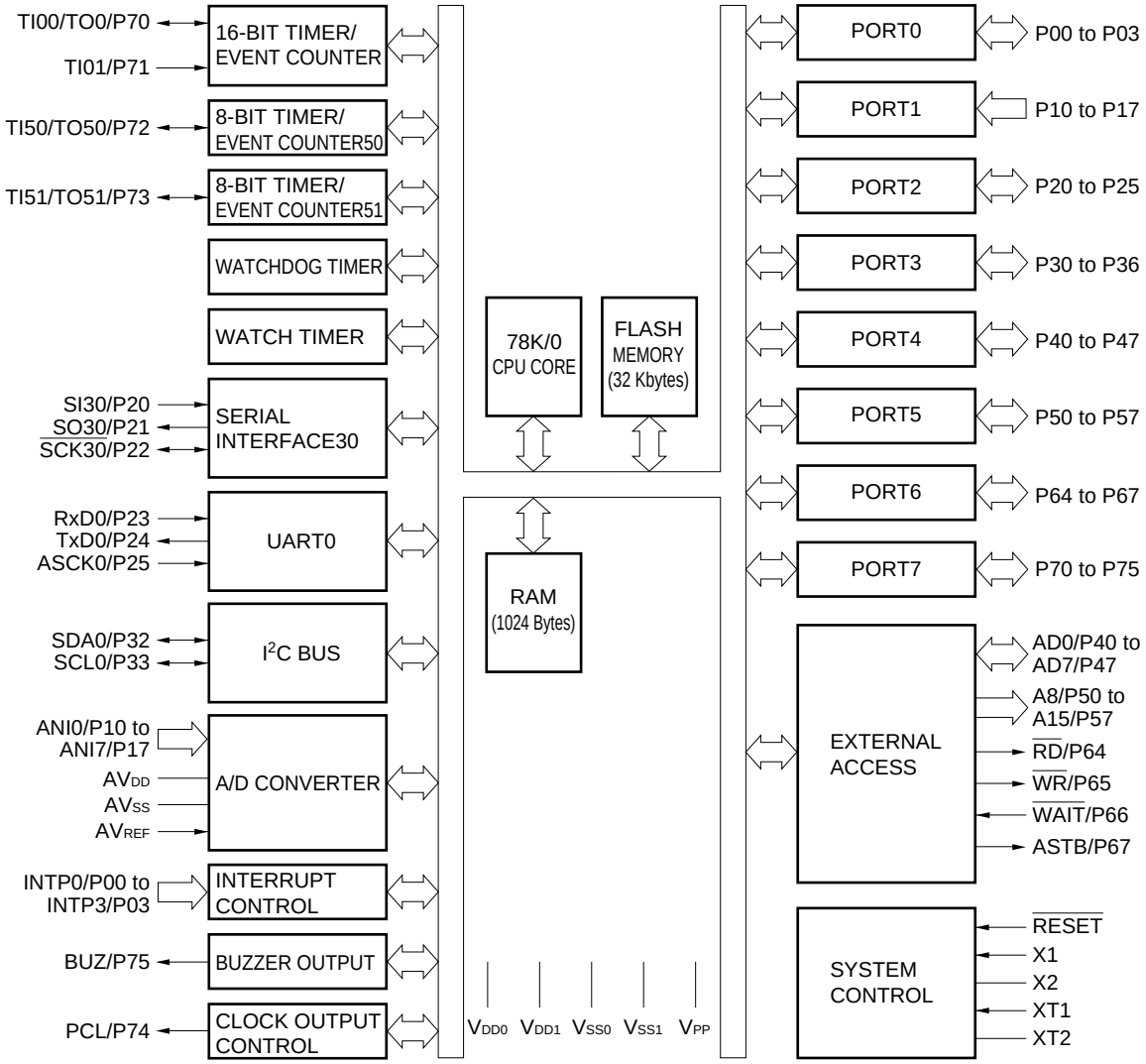
Cautions 1. Connect the V_{PP} pin directly to V_{SS0} or V_{SS1} in normal operation mode.

2. Connect the AV_{SS} pin to V_{SS0}.

Remark When the μPD78F0034AY is used in application fields that require reduction of the noise generated from inside the microcontroller, the implementation of noise reduction measures, such as supplying voltage to V_{DD0} and V_{DD1} individually and connecting V_{SS0} and V_{SS1} to different ground lines, is recommended.

A8 to A15:	Address Bus	PCL:	Programmable Clock
AD0 to AD7:	Address/Data Bus	$\overline{RD}$:	Read Strobe
ADTRG:	AD Trigger Input	$\overline{RESET}$:	Reset
ANI0 to ANI7:	Analog Input	RxD0:	Receive Data
ASCK0:	Asynchronous Serial Clock	$\overline{SCK30}$, SCL0:	Serial Clock
ASTB:	Address Strobe	SDA0:	Serial Data
AV_{DD}:	Analog Power Supply	SI30:	Serial Input
AV_{REF}:	Analog Reference Voltage	SO30:	Serial Output
AV_{SS}:	Analog Ground	TI00, TI01, TI50, TI51:	Timer Input
BUZ:	Buzzer Clock	TO0, TO50, TO51:	Timer Output
INTP0 to INTP3:	External Interrupt Input	TxD0:	Transmit Data
P00 to P03:	Port 0	V_{DD0}, V_{DD1}:	Power Supply
P10 to P17:	Port 1	V_{PP}:	Programming Power Supply
P20 to P25:	Port 2	V_{SS0}, V_{SS1}:	Ground
P30 to P36:	Port 3	$\overline{WAIT}$:	Wait
P40 to P47:	Port 4	$\overline{WR}$:	Write Strobe
P50 to P57:	Port 5	X1, X2:	Crystal (Main System Clock)
P64 to P67:	Port	XT1, XT2:	Crystal (Subsystem Clock)
P70 to P75:	Port 7		

BLOCK DIAGRAM



CONTENTS

1. DIFFERENCES BETWEEN μPD78F0034AY AND MASK ROM VERSIONS

The μPD78F0034AY is a product provided with a flash memory which enables writing, erasing, and rewriting of programs with device mounted on the target system.

The functions of the μPD78F0034AY (except the functions specified for flash memory) can be made the same as those of the mask ROM versions by setting the memory size switching register (IMS).

Table 1-1 shows the differences between the flash memory (μPD78F0034AY) and the mask ROM versions.

Table 1-1. Differences Between μPD78F0034AY and Mask ROM Versions

Item	μPD78F0034AY	Mask ROM Versions	
		μPD780034AY Subseries	μPD780024AY Subseries[Note]
Internal ROM structure	Flash memory	Mask ROM	
Internal ROM capacity	32 Kbytes	μPD780031AY: 8 Kbytes μPD780032AY: 16 Kbytes μPD780033AY: 24 Kbytes μPD780034AY: 32 Kbytes	μPD780021AY: 8 Kbytes μPD780022AY: 16 Kbytes μPD780023AY: 24 Kbytes μPD780024AY: 32 Kbytes
Internal high-speed RAM capacity	1024 bytes	μPD780031AY: 512 bytes μPD780032AY: 512 bytes μPD780033AY: 1024 bytes μPD780034AY: 1024 bytes	μPD780021AY: 512 bytes μPD780022AY: 512 bytes μPD780023AY: 1024 bytes μPD780024AY: 1024 bytes
A/D converter resolution	10 bits		8 bits
Mask option specification of on-chip pull-up resistor for pins P30 to P31	Not available	Available	
IC pin	Not provided	Provided	
V_{PP} pin	Provided	Not provided	
Electrical specifications, recommended soldering conditions	Refer to the data sheet of individual products.		

Note The μPD78F0034AY can be used as the flash memory version of the μPD780024AY Subseries.

Caution There are differences in noise immunity and noise radiation between the flash memory and mask ROM versions. When pre-producing an application set with the flash memory version and then mass producing it with the mask ROM version, be sure to conduct sufficient evaluations on the commercial samples (CS) (not engineering samples (ES)) of the mask ROM versions.

2. PIN FUNCTIONS

2.1 Port Pins (1/2)

Pin Name	I/O	Function		After Reset	Alternate Function
P00	I/O	Port 0 4-bit input/output port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software.		Input	INTP0
P01					INTP1
P02					INTP2
P03					INTP3/ADTRG
P10 to P17	Input	Port 1 8-bit input only port.		Input	ANI0 to ANI7
P20	I/O	Port 2 6-bit input/output port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software.		Input	SI30
P21					SO30
P22					$\overline{\text{SCK30}}$
P23					RxD0
P24					TxD0
P25					ASCK0
P30	I/O	Port 3 7-bit input/output port. Input/output can be specified in 1-bit units	N-ch open drain input/output port. LEDs can be driven directly.	Input	—
P31					
P32					SDA0
P33					SCL0
P34			An on-chip pull-up resistor can be specified by means of software.		—
P35					
P36					
P40 to P47	I/O	Port 4 8-bit input/output port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software. Interrupt request flag KRIF is set to 1 by falling edge detection.		Input	AD0 to AD7
P50 to P57	I/O	Port 5 8-bit input/output port. LEDs can be driven directly. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software.		Input	A8 to A15
P64	I/O	Port 6 4-bit input/output port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software.		Input	$\overline{\text{RD}}$
P65					$\overline{\text{WR}}$
P66					$\overline{\text{WAIT}}$
P67					ASTB

2.1 Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
P70	I/O	Port 7 6-bit input/output port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software.	Input	TI00/TO0
P71				TI01
P72				TI50/TO50
P73				TI51/TO51
P74				PCL
P75				BUZ

2.2 Non-Port Pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0 to INTP2	Input	External interrupt request input by which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.	Input	P00 to P02
INTP3				P03/ADTRG
SI30	Input	Serial interface serial data input.	Input	P20
SO30	Output	Serial interface serial data output.	Input	P21
SDA0	I/O	Serial interface serial data input/output.	Input	P32
$\overline{\text{SCK30}}$	I/O	Serial interface serial clock input/output.	Input	P22
SCL0				P33
RxD0	Input	Serial data input for asynchronous serial interface.	Input	P23
TxD0	Output	Serial data output for asynchronous serial interface.	Input	P24
ASCK0	Input	Serial clock input for asynchronous serial interface.	Input	P25
TI00	Input	External count clock input to 16-bit timer (TM0). Capture trigger signal input to TM0 capture register (CR01).	Input	P70/TO0
TI01		Capture trigger signal input to TM0 capture register (CR00).		P71
TI50		External count clock input to 8-bit timer (TM50).		P72/TO50
TI51		External count clock input to 8-bit timer (TM51).		P73/TO51
TO0	Output	16-bit timer (TM0) output.	Input	P70/TI00
TO50		8-bit timer (TM50) output (shared with 8-bit PWM output).	Input	P72/TI50
TO51		8-bit timer (TM51) output (shared with 8-bit PWM output).		P73/TI51
PCL	Output	Clock output (for trimming of main system clock and subsystem clock).	Input	P74
BUZ	Output	Buzzer output.	Input	P75
AD0 to AD7	I/O	Lower address/data bus for extending memory externally.	Input	P40 to P47
A8 to A15	Output	Higher address bus for extending memory externally.	Input	P50 to P57
$\overline{\text{RD}}$	Output	Strobe signal output for read operation of external memory.	Input	P64
$\overline{\text{WR}}$		Strobe signal output for write operation of external memory.		P65
$\overline{\text{WAIT}}$	Input	Inserting wait for accessing external memory.	Input	P66
ASTB	Output	Strobe output which externally latches address information output to ports 4 and 5 to access external memory.	Input	P67

2.2 Non-Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
ANI0 to ANI7	Input	A/D converter analog input.	Input	P10 to P17
ADTRG	Input	A/D converter trigger signal input.	Input	P03/INTP3
AV_{REF}	Input	A/D converter reference voltage input.	—	—
AV_{DD}	—	A/D converter analog power supply. Set the voltage equal to V_{DD0} or V_{DD1}.	—	—
AV_{SS}	—	A/D converter ground potential. Set the voltage equal to V_{SS0} or V_{SS1}.	—	—
$\overline{RESET}$	Input	System reset input.	—	—
X1	Input	Connecting crystal resonator for main system clock oscillation.	—	—
X2	—		—	—
XT1	Input	Connecting crystal resonator for subsystem clock oscillation.	—	—
XT2	—		—	—
V_{DD0}	—	Positive power supply voltage for ports.	—	—
V_{SS0}	—	Ground potential of ports.	—	—
V_{DD1}	—	Positive power supply (except ports).	—	—
V_{SS1}	—	Ground potential (except ports).	—	—
V_{PP}	—	Applying high-voltage for program write/verify. Connect directly to V_{SS0} or V_{SS1} in normal operation mode.	—	—

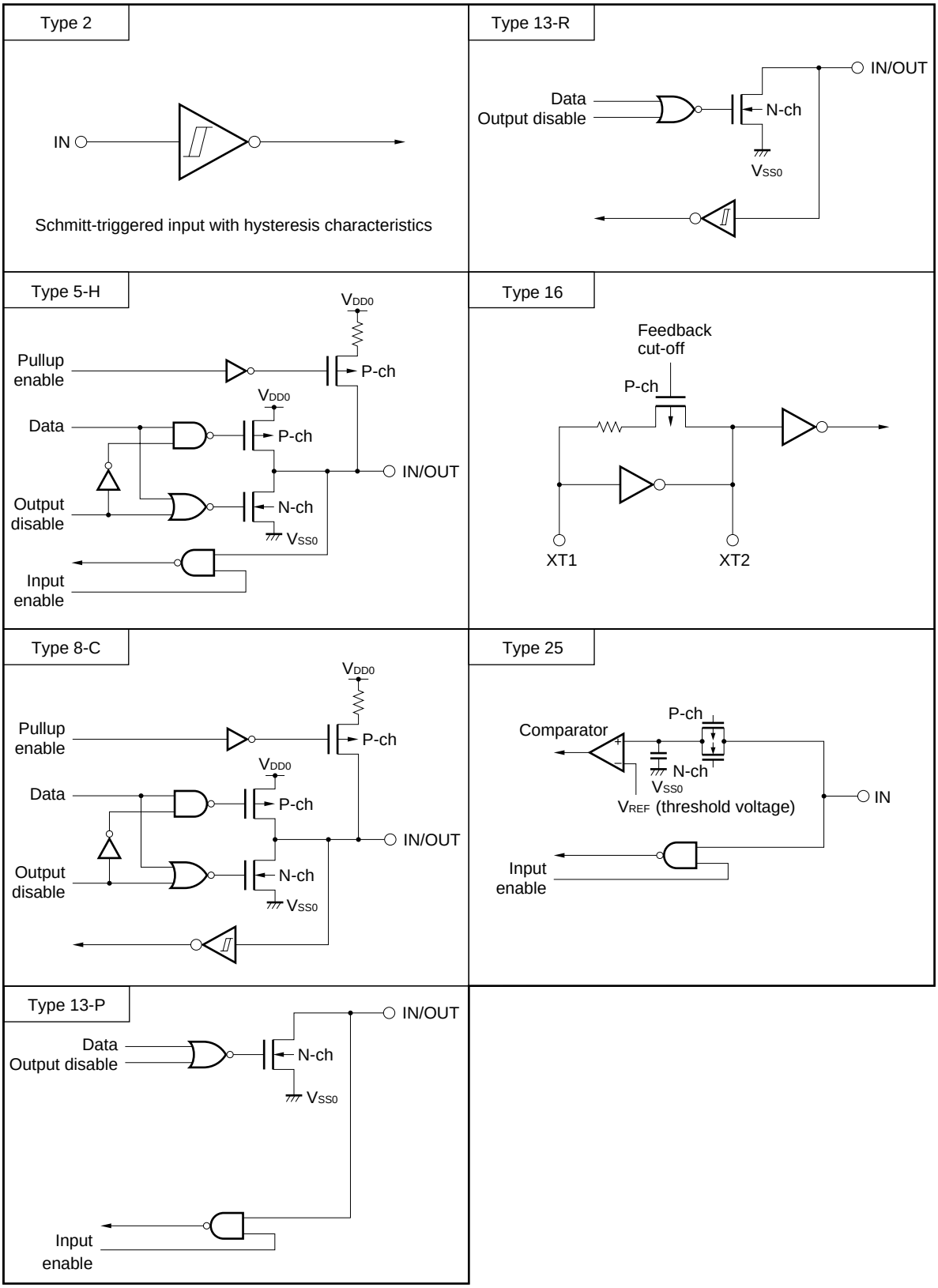
2.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 2-1. For the input/output configuration of each type, refer to Figure 2-1 .

Table 2-1. Types of Pin Input/Output Circuits

Pin Name	Input/Output Circuit Type	I/O	Recommended Connection of Unused Pins
P00/INTP0 to P02/INTP2	8-C	Input	Independently connect to V_{SS0} via a resistor.
P03/INTP3/ADTRG			
P10/ANI0 to P17/ANI7	25	Input	Independently connect to V_{DD0} or V_{SS0} via a resistor.
P20/SI30	8-C	Input/output	
P21/SO30	5-H		
P22/$\overline{\text{SCK30}}$	8-C		
P23/RxD0			
P24/TxD0	5-H		
P25/ASCK0	8-C		
P30, P31	13-P	Input/output	Independently connect to V_{DD0} via a resistor.
P32/SDA0	13-R		
P33/SCL0			
P34	8-C		Independently connect to V_{DD0} or V_{SS0} via a resistor.
P35	5-H		
P36	8-C		
P40/AD0 to P47/AD7	5-H	Input/output	Independently connect to V_{DD0} via a resistor.
P50/A8 to P57/A15	5-H	Input/output	Independently connect to V_{DD0} or V_{SS0} via a resistor.
P64/RD		Input/output	
P65/$\overline{\text{WR}}$			
P66/$\overline{\text{WAIT}}$			
P67/$\overline{\text{ASTB}}$			
P70/TI00/TO0	8-C		
P71/TI01			
P72/TI50/TO50			
P73/TI51/TO51			
P74/PCL	5-H		
P75/BUZ			
$\overline{\text{RESET}}$	2	Input	—
XT1	16		Connect to V_{DD0}.
XT2		—	Leave open.
AV_{DD}	—		Connect to V_{DD0}.
AV_{REF}			Connect to V_{SS0}.
AV_{SS}			
V_{PP}			Connect directly to V_{SS0} or V_{SS1}.

Figure 2-1. Pin Input/Output Circuits



3. MEMORY SIZE SWITCHING REGISTER (IMS)

IMS is a register that is set by software and is used to specify a part of the internal memory that is not to be used. By setting IMS, the internal memory of the μPD78F0034AY can be mapped identically to that of a mask ROM version.

IMS is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets the IMS to CFH.

Caution The initial value of IMS is setting disabled (CFH). Be sure to set C8H or the value of the target mask ROM version at the moment of initial setting.

Figure 3-1. Format of Memory Size Switching Register

	7	6	5	4	3	2	1	0	Address	After reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	CFH	R/W

ROM3	ROM2	ROM1	ROM0	Selection of Internal ROM Capacity
0	0	1	0	8 Kbytes
0	1	0	0	16 Kbytes
0	1	1	0	24 Kbytes
1	0	0	0	32 Kbytes
Other than above				Setting prohibited

RAM2	RAM1	RAM0	Selection of Internal High-Speed RAM Capacity
0	1	0	512 bytes
1	1	0	1024 bytes
Other than above			Setting prohibited

Table 3-1 shows the IMS set value to make the memory mapping the same as those of mask ROM versions.

Table 3-1. Set Value of Memory Size Switching Register

Target Mask ROM Versions	IMS Set Value
μPD780031AY	42H
μPD780032AY	44H
μPD780033AY	C6H
μPD780034AY	C8H

4. FLASH MEMORY PROGRAMMING

Writing to flash memory can be performed without removing the memory from the target system (on board programming). Writing is performed with the dedicated flash programmer (Flashpro II (model No.: FL-PR2) or Flashpro III (model No.: FL-PR3 and PG-FP3)) connected to the host machine and the target system.

Writing to flash memory can also be performed using flash memory writing adapter connected to Flashpro II or Flashpro III.

Remark FL-PR2 and FL-PR3 are products of Naito Densei Machida Mfg. Co., Ltd.

4.1 Selection of Communication Mode

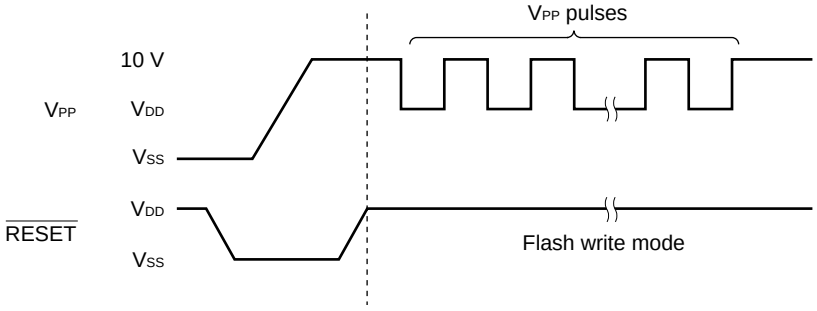
Writing to a flash memory is performed using Flashpro II or Flashpro III in a serial communication. Select one of the communication modes in Table 4-1. The selection of the communication mode is made by using the format shown in Figure 4-1. Each communication mode is selected by the number of V_{PP} pulses shown in Table 4-1.

Table 4-1. List of Communication Mode

Communication Mode	Channels	Used Pin	V_{PP} Pulses
3-wire serial I/O	1	SI30/P20 SO30/P21 $\overline{\text{SCK30}}$/P22	0
I^2C bus	1	SDA0/P32 SCL0/P33	4
UART	1	RxD0/P23 TxD0/P24	8
Pseudo 3-wire serial I/O	1	P72/TI50/TO50 (serial clock input) P71/TI01 (serial data output) P70/TI00/TO0 (serial data input)	12

Caution Be sure to select a communication mode using the number of V_{PP} pulses shown in Table 4-1.

Figure 4-1. Format of Communication Mode Selection



4.2 Flash Memory Programming Functions

Operations such as writing to flash memory are performed by various command/data transmission and reception operations according to the selected communication mode. Table 4-2 shows major functions of flash memory programming.

Table 4-2. Major Functions of Flash Memory Programming

Function	Description
Reset	Used to stop write operation and detect transmission cycle.
Batch verify	Compares the entire memory contents with the input data.
Batch erase	Erases the entire memory contents.
Batch blank check	Checks the deletion status of the entire memory.
High-speed write	Performs write to the flash memory based on the write start address and the number of data to be written (number of bytes).
Continuous write	Performs continuous write based on the information input with high-speed write operation.
Status	Used to confirm the current operating mode and operation end.
Oscillation frequency setting	Sets the frequency of the resonator.
Erase time setting	Sets the memory erase time.
Silicon signature read	Outputs the device name and memory capacity, and device block information.

4.3 Connection of Flashpro II and Flashpro III

The connection of Flashpro II or Flashpro III and the μPD78F0034AY differs according to the communication mode (3-wire serial I/O, UART, and pseudo 3-wire serial I/O). The connection for each communication mode is shown in Figures 4-2 through 4-5, respectively.

Figure 4-2. Connection of Flashpro II or Flashpro III for 3-Wire Serial I/O Mode

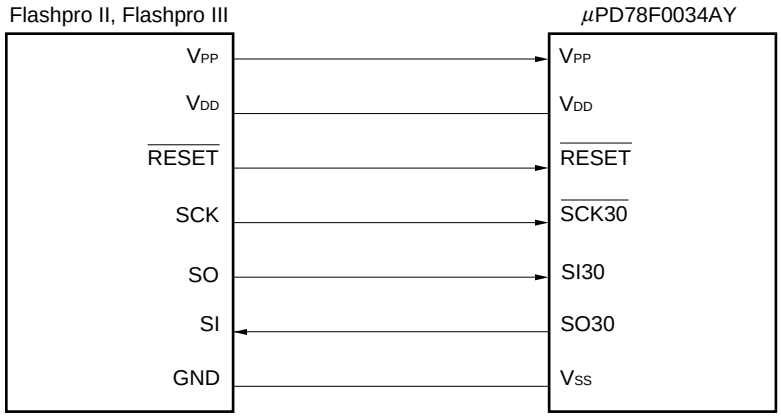


Figure 4-3. Connection of Flashpro II or Flashpro III for I²C Bus Mode

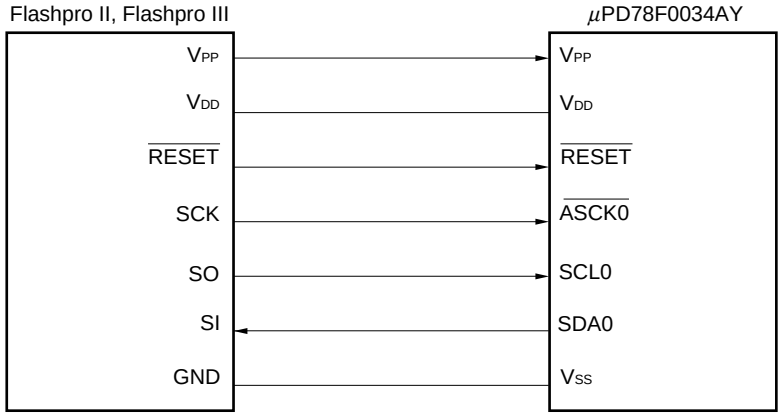


Figure 4-4. Connection of Flashpro II or Flashpro III for UART Mode

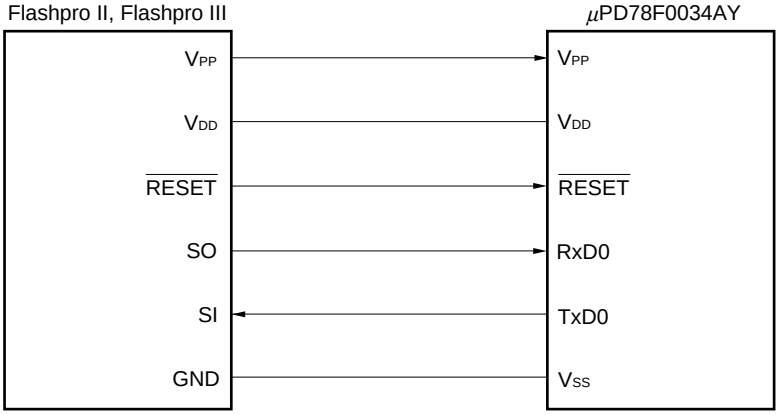
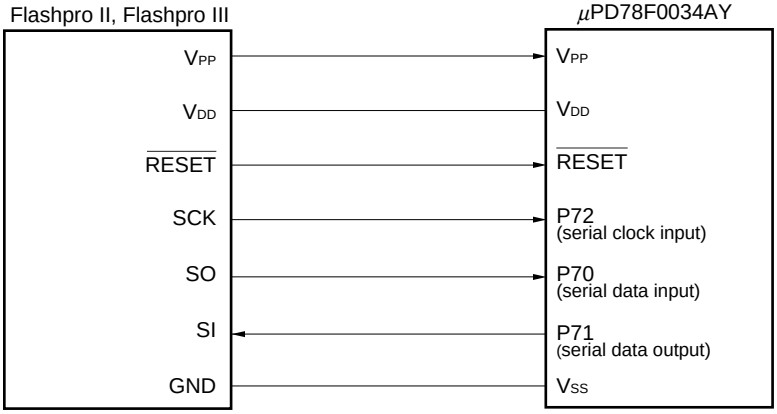


Figure 4-5. Connection of Flashpro II or Flashpro III for Pseudo 3-Wire Serial I/O Mode



5. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Test Conditions		Ratings	Unit
Supply voltage	V_{DD}			–0.3 to +6.5	V
	V_{PP}			–0.3 to +10.5	V
	AV_{DD}			–0.3 to V_{DD} + 0.3[Note]	V
	AV_{REF}			–0.3 to V_{DD} + 0.3[Note]	V
	AV_{SS}			–0.3 to +0.3	V
Input voltage	V_{I1}	P00 to P03, P10 to P17,P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, X1, X2, XT1, XT2, $\overline{\text{RESET}}$		–0.3 to V_{DD} + 0.3[Note]	V
	V_{I2}	P30 to P33	N-ch open drain	–0.3 to +6.5	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3[Note]	V
Analog input voltage	V_{AN}	P10 to P17	Analog input pin	AV_{SS} –0.3 to AV_{REF} + 0.3[Note] and –0.3 to V_{DD} + 0.3[Note]	V
Output current, high	I_{OH}	Per pin		–10	mA
		Total for P00 to P03, P40 to P47, P50 to P57, P64 to P67, P70 to P75		–15	mA
		Total for P20 to P25, P30 to P36		–15	mA
Output current, low	I_{OL}	Per pin for P00 to P03, P20 to P25, P34 to P36, P40 to P47, P64 to P67, P70 to P75		20	mA
		Per pin for P30 to P33, P50 to P57		30	mA
		Total for P00 to P03, P40 to P47, P64 to P67, P70 to P75		50	mA
		Total for P20 to P25		20	mA
		Total for P30 to P36		100	mA
		Total for P50 to P57		100	mA
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–40 to +125	°C

Note The rating should be 6.5 V or less.

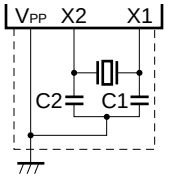
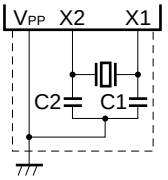
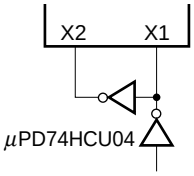
Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Pins other than measured pins returned to 0 V.				15	pF
I/O capacitance	C_{IO}	f = 1 MHz Pins other than measured pins returned to 0 V.	P00 to P03, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75,			15	pF
			P30 to P33			20	pF

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Main System Clock Oscillation Circuit Characteristics (T_A = –40 to 85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)**Note 1**	V_{DD} = 4.0 to 5.5 V	1.0		8.38	MHz
				1.0		5.0	
		Oscillation stabilization time**Note 2**	After V_{DD} reaches oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequency (f_X)**Note 1**	V_{DD} = 4.0 to 5.5 V	1.0		8.38	MHz
				1.0		5.0	
		Oscillation stabilization time**Note 2**	V_{DD} = 4.0 to 5.5 V			10	ms
						30	
External clock		X1 input frequency (f_X)**Note 1**	V_{DD} = 4.0 to 5.5 V	1.0		8.38	MHz
				1.0		5.0	
		X1 input high-/low-level width (t_{XH}, t_{XL})	V_{DD} = 4.0 to 5.5 V	50		500	ns
				85		500	

Notes 1. Indicates only oscillation circuit characteristics. Refer to **AC Characteristics** for instruction execution time.

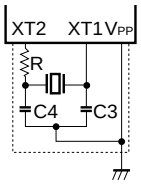
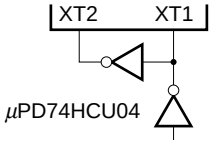
2. Time required to stabilize oscillation after reset or STOP mode release.

Cautions 1. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always keep the ground point of the oscillator capacitor the same potential as V_{SS1}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched again to the main system clock after the oscillation stabilization time is secured by the program.

Subsystem Clock Oscillation Circuit Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})**Note 1**		32	32.768	35	kHz
		Oscillation stabilization time**Note 2**	V_{DD} = 4.0 to 5.5 V		1.2	2	s
						10	
External clock		X1 input frequency (f_{XT})**Note 1**		32		38.5	kHz
		X1 input high-/low-level width (t_{XTH}, t_{XTL})		5		15	μs

Notes 1. Indicates only oscillation circuit characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after V_{DD} reaches oscillator voltage MIN.

Cautions 1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken line in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always keep the ground point of the oscillator to the same potential as V_{SS1}.**
- **Do not ground the capacitor to a ground pattern in which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subsystem clock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

Recommended Oscillator Constant

Main System Clock: Ceramic Resonator (T_A = –40 to +85°C)

Manufacturer	Part Number	Frequency	Recommended Circuit Constant		Oscillation Voltage Range	
		(MHz)	C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)
Murata Mfg. Co., Ltd.	CSB1000J	1.00	100	100	1.9	5.5
	CSA2.00MG040	2.00	100	100	2.0	5.5
	CST2.00MG040	2.00	On-chip	On-chip	2.0	5.5
	CSA3.58MG	3.58	30	30	2.0	5.5
	CST3.58MGW	3.58	On-chip	On-chip	2.0	5.5
	CSA3.58MG093	3.58	30	30	1.8	5.5
	CST3.58MGW093	3.58	On-chip	On-chip	1.8	5.5
	CSA4.19MG	4.19	30	30	2.0	5.5
	CST4.19MGW	4.19	On-chip	On-chip	2.0	5.5
	CSA4.19MG093	4.19	30	30	1.8	5.5
	CST4.19MGW093	4.19	On-chip	On-chip	1.8	5.5
	CSA5.00MG	5.00	30	30	2.0	5.5
	CST5.00MGW	5.00	On-chip	On-chip	2.0	5.5
	CSA5.00MG093	5.00	30	30	1.8	5.5
	CST5.00MGW093	5.00	On-chip	On-chip	1.8	5.5
	CSA8.00MTZ	8.00	30	30	4.0	5.5
	CST8.00MTW	8.00	On-chip	On-chip	4.0	5.5
	CSA8.00MTZ093	8.00	30	30	4.0	5.5
	CST8.00MTW093	8.00	On-chip	On-chip	4.0	5.5
	CSA8.38MTZ	8.38	30	30	4.0	5.5
	CST8.38MTW	8.38	On-chip	On-chip	4.0	5.5
	CSA8.38MTZ093	8.38	30	30	4.0	5.5
	CST8.38MTW093	8.38	On-chip	On-chip	4.0	5.5
TDK	CCR3.58MC3	3.58	On-chip	On-chip	1.8	5.5
	CCR4.19MC3	4.19	On-chip	On-chip	1.8	5.5
	CCR5.0MC3	5.00	On-chip	On-chip	1.8	5.5
	CCR8.0MC5	8.00	On-chip	On-chip	4.0	5.5
	CCR8.38MC5	8.38	On-chip	On-chip	4.0	5.5

Caution The oscillator constant and oscillation voltage range indicate conditions of stable oscillation. Oscillation frequency precision is not guaranteed. For applications requiring oscillation frequency precision, the oscillation frequency must be adjusted on the implementation circuit. For details please contact directly the manufacturer of the resonator you will use.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high	I_{OH}	Per pin				–1	mA
		All pins				–15	mA
Output current, low	I_{OL}	Per pin for P00 to P03, P20 to P25, P34 to P36, P40 to P47, P64 to P67, P70 to P75				10	mA
		Per pin for P30 to P33, P50 to P57				15	mA
		Total for P00 to P03, P40 to P47, P64 to P67, P70 to P75				20	mA
		Total for P20 to P25				10	mA
		Total for P30 to P36				70	mA
		Total for P50 to P57				70	mA
Input voltage, high	V_{IH1}	P10 to P17, P21, P24, P35, P40 to P47, P50 to P57, P64 to P67, P74, P75	V_{DD} = 2.7 to 5.5 V	0.7 V_{DD}		V_{DD}	V
				0.8 V_{DD}		V_{DD}	V
	V_{IH2}	P00 to P03, P20, P22, P23, P25, P34, P36, P70 to P73, $\overline{\text{RESET}}$	V_{DD} = 2.7 to 5.5 V	0.8 V_{DD}		V_{DD}	V
				0.85 V_{DD}		V_{DD}	V
	V_{IH3}	P30 to P33 (N-ch open-drain)	V_{DD} = 2.7 to 5.5 V	0.7 V_{DD}		5.5	V
				0.8 V_{DD}		5.5	V
	V_{IH4}	X1, X2	V_{DD} = 2.7 to 5.5 V	V_{DD}–0.5		V_{DD}	V
				V_{DD}–0.2		V_{DD}	V
	V_{IH5}	XT1, XT2	V_{DD} = 4.0 to 5.5 V	0.8 V_{DD}		V_{DD}	V
				0.9 V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P10 to P17, P21, P24, P35, P40 to P47, P50 to P57, P64 to P67, P74, P75	V_{DD} = 2.7 to 5.5 V	0		0.3 V_{DD}	V
				0		0.2 V_{DD}	V
	V_{IL2}	P00 to P03, P20, P22, P23, P25, P34, P36, P70 to P73, $\overline{\text{RESET}}$	V_{DD} = 2.7 to 5.5 V	0		0.2 V_{DD}	V
				0		0.15 V_{DD}	V
	V_{IL3}	P30 to P33	4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.3 V_{DD}	V
			2.7 V ≤ V_{DD} < 4.0 V	0		0.2 V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7	0		0.1 V_{DD}	V
	V_{IL4}	X1, X2	V_{DD} = 2.7 to 5.5 V	0		0.4	V
				0		0.2	V
	V_{IL5}	XT1, XT2	V_{DD} = 4.0 to 5.5 V	0		0.2 V_{DD}	V
				0		0.1 V_{DD}	V
Output voltage, high	V_{OH1}	V_{DD} = 4.0 to 5.5 V, I_{OH} = –1 mA		V_{DD}–1.0		V_{DD}	V
		I_{OH} = –100 μA		V_{DD}–0.5		V_{DD}	V
Output voltage, low	V_{OL1}	P30 to P33	V_{DD} = 4.0 to 5.5 V, I_{OL} = 15 mA			2.0	V
		P50 to P57			0.4	2.0	V
		P00 to P03, P20 to P25, P34 to P36, P40 to P47, P64 to P67, P70 to P75	V_{DD} = 4.0 to 5.5 V, I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	I_{OL} = 400 μA				0.5	V

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	$V_{IN} = V_{DD}$	P00 to P03, P10 to P17, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, $\overline{\text{RESET}}$			3	μA
	I_{LIH2}		X1, X2, XT1, XT2			20	μA
	I_{LIH3}	V_{IN} = 5.5 V	P30 to P33			3	μA
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	P00 to P03, P10 to P17, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, $\overline{\text{RESET}}$			–3	μA
	I_{LIL2}		X1, X2, XT1, XT2			–20	μA
	I_{LIL3}		P30 to P33			–3	μA
Output leakage current, low	I_{LOH}	$V_{OUT} = V_{DD}$				3	μA
Output leakage current, low	I_{LOL}	V_{OUT} = 0 V				–3	μA
Software pull-up resistor	R	V_{IN} = 0 V, P00 to P03, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75		15	30	90	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins .

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD1}	8.38-MHz crystal oscillation operating mode	V_{DD} = 5.0 V ± 10 %[Note 2]	A/D converter stopped		10.5	21	mA
				A/D converter operating		11.5	23	mA
		5.00-MHz crystal oscillation operation mode	V_{DD} = 3.0 V ± 10 %[Note 2]	A/D converter stopped		4.5	9	mA
				A/D converter operating		5.5	11	mA
			V_{DD} = 2.0 V 10%[Note 3]	A/D converter stopped		1	2	mA
				A/D converter operating		2	6	mA
	I_{DD2}	8.38-MHz crystal oscillation HALT mode	V_{DD} = 5.0 V ± 10 %[Note 2]	Peripheral functions stopped		1.2	2.4	mA
				Peripheral functions operating			5	mA
		5.00-MHz crystal oscillation HALT mode	V_{DD} = 3.0 V ± 10 %[Note 2]	Peripheral functions stopped		0.4	0.8	mA
				Peripheral functions operating			1.7	mA
			V_{DD} = 2.0 V ± 10 %[Note 3]	Peripheral functions stopped		0.2	0.4	mA
				Peripheral functions operating			1.1	mA
	I_{DD3}	32.768-kHz crystal oscillation operating mode[Note 4]		V_{DD} = 5.0 V ± 10%[Note 2]		115	230	μA
				V_{DD} = 3.0 V ± 10%[Note 2]		95	190	μA
				V_{DD} = 2.0 V ± 10%[Note 3]		75	150	μA
	I_{DD4}	32.768-kHz crystal oscillation HALT mode[Note 4]		V_{DD} = 5.0 V ± 10%[Note 2]		30	60	μA
				V_{DD} = 3.0 V ± 10%[Note 2]		6	18	μA
				V_{DD} = 2.0 V ± 10%[Note 3]		2	10	μA
	I_{DD5}	XT1 = 0 V, STOP mode When feed-back resistor not used		V_{DD} = 5.0 V ± 10%[Note 2]		0.1	30	μA
				V_{DD} = 3.0 V ± 10%[Note 2]		0.05	10	μA
				V_{DD} = 2.0 V ± 10%[Note 3]		0.05	10	μA

Notes 1. Refers to the total current flowing through the internal power supply (V_{DD0} and V_{DD1}). Includes peripheral operating current (however, current flowing through the pull-up resistors of ports and the AV_{REF} pin is not included).

2. When the processor clock control register (PCC) is set to 00H.

3. When PCC is set to 02H.

4. When the main system clock is stopped.

AC Characteristics

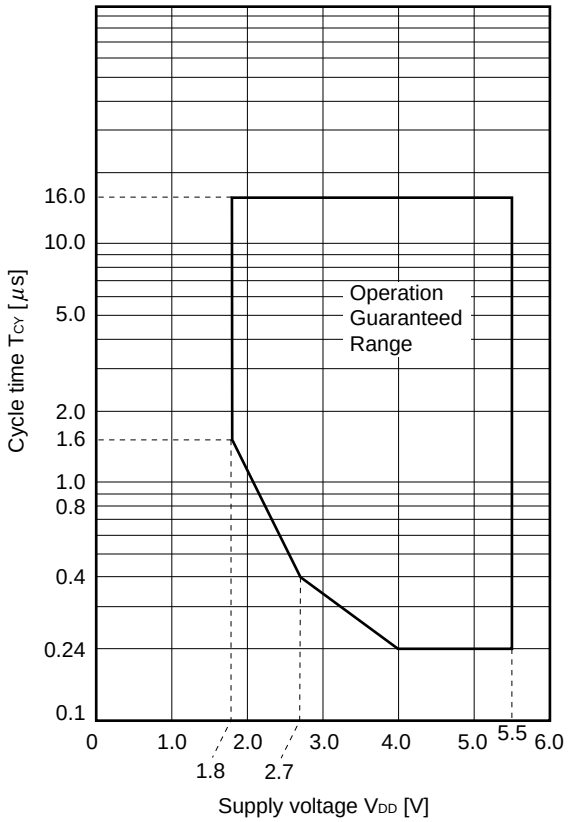
(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (Min. instruction execution time)	T_{CY}	Operating on main system clock	4.0 ≤ V_{DD} ≤ 5.5 V	0.24		16	μs
			2.7 V ≤ V_{DD} < 4.0 V	0.4		16	μs
				1.6		16	μs
		Operating on subsystem clock		103.9 Note 1	122	125	μs
TI00, TI01 input high-/low-level width	t_{TIH0}, t_{TIL0}	4.0 V ≤ V_{DD} ≤ 5.5 V		$2/f_{sam}$ + 0.1 Note 2			μs
		2.7 V ≤ V_{DD} < 4.0 V		$2/f_{sam}$ + 0.2 Note 2			μs
				$2/f_{sam}$ + 0.5 Note 2			μs
TI50, TI51 input frequency	f_{TI5}	V_{DD} = 2.7 to 5.5 V		0		4	MHz
				0		275	kHz
TI50, TI51 input high-/low-level width	t_{TIH5}, t_{TIL5}	V_{DD} = 2.7 to 5.5 V		100			ns
				1.8			μs
Interrupt request input high-/low -level width	t_{INTH}, t_{INTL}	INTP0 to INTP3, P40 to P47	V_{DD} = 2.7 to 5.5 V	1			μs
				2			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}	V_{DD} = 2.7 to 5.5 V		10			μs
				20			μs

Notes 1. Value when using an external clock. When using a crystal resonator, the value becomes 114 μs (MIN.).

2. Selection of $f_{sam} = f_X$, $f_X/4$, $f_X/64$ is possible using bits 0 and 1 (PRM00, PRM01) of prescaler mode register 0 (PRM0). However, if the TI00 valid edge is selected as the count clock, the value becomes $f_{sam} = f_X/8$.

T_{CY} vs V_{DD} (main system clock)



(2) Read/write operation (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V) (1/3)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.3t_{CY}$		ns
Address setup time	t_{ADS}		20		ns
Address hold time	t_{ADH}		6		ns
Data input time from address	t_{ADD1}			$(2 + 2n)t_{CY}$ – 54	ns
	t_{ADD2}			$(3 + 2n)t_{CY}$ – 60	ns
Address output time from $\overline{RD}\downarrow$	t_{RDAD}		0	100	ns
Data input time from $\overline{RD}\downarrow$	t_{RDD1}			$(2 + 2n)t_{CY}$ – 87	ns
	t_{RDD2}			$(3 + 2n)t_{CY}$ – 93	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		$(1.5 + 2n)t_{CY}$ – 33		ns
	t_{RDL2}		$(2.5 + 2n)t_{CY}$ – 33		ns
$\overline{WAIT}\downarrow$ input time from $\overline{RD}\downarrow$	t_{RDWT1}			t_{CY} – 43	ns
	t_{RDWT2}			t_{CY} – 43	ns
$\overline{WAIT}\downarrow$ input time from $\overline{WR}\downarrow$	t_{WRWT}			t_{CY} – 25	ns
$\overline{WAIT}$ low-level width	t_{WTL}		$(0.5 + n)t_{CY}$ + 10	$(2 + 2n)t_{CY}$	ns
Write data setup time	t_{WDS}		60		ns
Write data hold time	t_{WDH}		6		ns
$\overline{WR}$ low-level width	t_{WRL1}		$(1.5 + 2n)t_{CY}$ – 15		ns
$\overline{RD}\downarrow$ delay time from ASTB↓	t_{ASTRD}		6		ns
$\overline{WR}\downarrow$ delay time from ASTB↓	t_{ASTWR}		$2t_{CY}$ – 15		ns
ASTB↑ delay time from $\overline{RD}\uparrow$ in external fetch	t_{RDAST}		$0.8t_{CY}$ – 15	$1.2t_{CY}$	ns
Address hold time from $\overline{RD}\uparrow$ in external fetch	t_{RDADH}		$0.8t_{CY}$ – 15	$1.2t_{CY}$ + 30	ns
Write data output time from $\overline{RD}\uparrow$	t_{RDWD}		40		ns
Write data output time from $\overline{WR}\downarrow$	t_{WRWD}		10	60	ns
Address hold time from $\overline{WR}\uparrow$	t_{WRADH}		$0.8t_{CY}$ – 15	$1.2t_{CY}$ + 30	ns
$\overline{RD}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTRD}		$0.8t_{CY}$	$2.5t_{CY}$ + 25	ns
$\overline{WR}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTWR}		$0.8t_{CY}$	$2.5t_{CY}$ + 25	ns

Remarks 1. $t_{CY} = T_{CY}/4$

2. n indicates the number of waits.

3. C_L = 100 pF (C_L is the load capacitance of the AD0 to AD7, A8 to A15, $\overline{RD}$, $\overline{WR}$, $\overline{WAIT}$, and ASTB pins.)

(2) Read/write operation (T_A = –40 to +85°C, V_{DD} = 2.7 to 4.0 V) (2/3)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.3t_{CY}$		ns
Address setup time	t_{ADS}		30		ns
Address hold time	t_{ADH}		10		ns
Data input time from address	t_{ADD1}			$(2 + 2n)t_{CY}$ – 108	ns
	t_{ADD2}			$(3 + 2n)t_{CY}$ – 120	ns
Address output time from $\overline{RD}\downarrow$	t_{RDAD}		0	200	ns
Data input time from $\overline{RD}\downarrow$	t_{RDD1}			$(2 + 2n)t_{CY}$ – 148	ns
	t_{RDD2}			$(3 + 2n)t_{CY}$ – 162	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		$(1.5 + 2n)t_{CY}$ – 40		ns
	t_{RDL2}		$(2.5 + 2n)t_{CY}$ – 40		ns
$\overline{WAIT}\downarrow$ input time from $\overline{RD}\downarrow$	t_{RDWT1}			t_{CY} – 75	ns
	t_{RDWT2}			t_{CY} – 60	ns
$\overline{WAIT}\downarrow$ input time from $\overline{WR}\downarrow$	t_{WRWT}			t_{CY} – 50	ns
$\overline{WAIT}$ low-level width	t_{WTL}		$(0.5 + 2n)t_{CY}$ + 10	$(2 + 2n)t_{CY}$	ns
Write data setup time	t_{WDS}		60		ns
Write data hold time	t_{WDH}		10		ns
$\overline{WR}$ low-level width	t_{WRL1}		$(1.5 + 2n)t_{CY}$ – 30		ns
$\overline{RD}\downarrow$ delay time from ASTB$\downarrow$	t_{ASTRD}		10		ns
$\overline{WR}\downarrow$ delay time from ASTB$\downarrow$	t_{ASTWR}		$2t_{CY}$ – 30		ns
ASTB$\uparrow$ delay time from $\overline{RD}\uparrow$ in external fetch	t_{RDAST}		$0.8t_{CY}$ – 30	$1.2t_{CY}$	ns
Address hold time from $\overline{RD}\uparrow$ in external fetch	t_{RDADH}		$0.8t_{CY}$ – 30	$1.2t_{CY}$ + 60	ns
Write data output time from $\overline{RD}\uparrow$	t_{RDWD}		40		ns
Write data output time from $\overline{WR}\downarrow$	t_{WRWD}		20	120	ns
Address hold time from $\overline{WR}\uparrow$	t_{WRADH}		$0.8t_{CY}$ – 30	$1.2t_{CY}$ + 60	ns
$\overline{RD}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTRD}		$0.5t_{CY}$	$2.5t_{CY}$ + 50	ns
$\overline{WR}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTWR}		$0.5t_{CY}$	$2.5t_{CY}$ + 50	ns

Remarks 1. $t_{CY} = T_{CY}/4$

2. n indicates the number of waits.

3. C_L = 100 pF (C_L is the load capacitance of the AD0 to AD7, A8 to A15, $\overline{RD}$, $\overline{WR}$, $\overline{WAIT}$, and ASTB pins.)

(2) Read/write operation (T_A = –40 to +85°C, V_{DD} = 1.8 to 2.7 V) (3/3)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.3t_{CY}$		ns
Address setup time	t_{ADS}		120		ns
Address hold time	t_{ADH}		20		ns
Data input time from address	t_{ADD1}			$(2 + 2n)t_{CY}$ – 233	ns
	t_{ADD2}			$(3 + 2n)t_{CY}$ – 240	ns
Address output time from $\overline{RD}\downarrow$	t_{RDAD}		0	400	ns
Data input time from $\overline{RD}\downarrow$	t_{RDD1}			$(2 + 2n)t_{CY}$ – 325	ns
	t_{RDD2}			$(3 + 2n)t_{CY}$ – 332	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		$(1.5 + 2n)t_{CY}$ – 92		ns
	t_{RDL2}		$(2.5 + 2n)t_{CY}$ – 92		ns
$\overline{WAIT}\downarrow$ input time from $\overline{RD}\downarrow$	t_{RDWT1}			t_{CY} – 350	ns
	t_{RDWT2}			t_{CY} – 132	ns
$\overline{WAIT}\downarrow$ input time from $\overline{WR}\downarrow$	t_{WRWT}			t_{CY} – 100	ns
$\overline{WAIT}$ low-level width	t_{WTL}		$(0.5 + 2n)t_{CY}$ + 10	$(2 + 2n)t_{CY}$	ns
Write data setup time	t_{WDS}		60		ns
Write data hold time	t_{WDH}		20		ns
$\overline{WR}$ low-level width	t_{WRL1}		$(1.5 + 2n)t_{CY}$ – 60		ns
$\overline{RD}\downarrow$ delay time from ASTB$\downarrow$	t_{ASTRD}		20		ns
$\overline{WR}\downarrow$ delay time from ASTB$\downarrow$	t_{ASTWR}		$2t_{CY}$ – 60		ns
ASTB$\uparrow$ delay time from $\overline{RD}\uparrow$ at external fetch	t_{RDAST}		$0.8t_{CY}$ – 60	$1.2t_{CY}$	ns
Address hold time from $\overline{RD}\uparrow$ at external fetch	t_{RDADH}		$0.8t_{CY}$ – 60	$1.2t_{CY}$ + 120	ns
Write data output time from $\overline{RD}\uparrow$	t_{RDWD}		40		ns
Write data output time from $\overline{WR}\downarrow$	t_{WRWD}		40	240	ns
Address hold time from $\overline{WR}\uparrow$	t_{WRADH}		$0.8t_{CY}$ – 60	$1.2t_{CY}$ + 120	ns
$\overline{RD}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTRD}		$0.5t_{CY}$	$2.5t_{CY}$ + 100	ns
$\overline{WR}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTWR}		$0.5t_{CY}$	$2.5t_{CY}$ + 100	ns

Remarks 1. $t_{CY} = T_{CY}/4$

2. n indicates the number of waits.

3. C_L = 100 pF (C_L is the load capacitance of the AD0 to AD7, A8 to A15, $\overline{RD}$, $\overline{WR}$, $\overline{WAIT}$, and ASTB pins.)

(3) Serial interface (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

(a) 3-wire serial I/O mode ($\overline{SCK30}$... internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK30}$ cycle time	t_{KCY1}	4.0 V ≤ V_{DD} ≤ 5.5 V	954			ns
		2.7 V ≤ V_{DD} < 4.0 V	1600			ns
			3200			ns
$\overline{SCK30}$ high-/low-level width	t_{KH1}, t_{KL1}	V_{DD} = 4.0 to 5.5 V	t_{KCY1}/2–50			ns
			t_{KCY1}/2–100			ns
SI30 setup time (to $\overline{SCK30}$)	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.0 V	150			ns
			300			ns
SI30, SI31 hold time (from $\overline{SCK30}$)	t_{KSI1}		400			ns
S030 output delay time from $\overline{SCK30}$	t_{KSO1}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of the $\overline{SCK30}$ and SO30 output lines.

(b) 3-wire serial I/O mode ($\overline{SCK30}$... external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK30}$ cycle time	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.0 V	1600			ns
			3200			ns
$\overline{SCK30}$ high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ V_{DD} ≤ 5.5 V	400			ns
		2.7 V ≤ V_{DD} < 4.0 V	800			ns
			1600			ns
SI30 setup time (to $\overline{SCK30}$)	t_{SIK2}		100			ns
SI30, SI31 hold time (from $\overline{SCK30}$)	t_{KSI2}		400			ns
SO30 output delay time from $\overline{SCK30}$	t_{KSO2}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of the SO30 output line.

(c) UART mode (Dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		4.0 V ≤ V_{DD} ≤ 5.5 V			131031	bps
		2.7 V ≤ V_{DD} < 4.0 V			78125	bps
					39063	bps

(d) UART mode (External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK0 cycle time	t_{KCY3}	4.0 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.0 V	1600			ns
			3200			ns
ASCK0 high-/low-level width	t_{KH3}, t_{KL3}	4.0 V ≤ V_{DD} ≤ 5.5 V	400			ns
		2.7 V ≤ V_{DD} < 4.0 V	800			ns
			1600			ns
Transfer rate		4.0 V ≤ V_{DD} ≤ 5.5 V			39063	bps
		2.7 V ≤ V_{DD} < 4.0 V			19531	bps
					9766	bps

(e) UART mode (Infrared data transfer mode)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Transfer rate		V_{DD} = 4.0 to 5.5 V		131031	bps
Bit rate allowable error		V_{DD} = 4.0 to 5.5 V		±0.87	%
Output pulse width		V_{DD} = 4.0 to 5.5 V	1.2	0.24/fbr**Note**	μs
Input pulse width		V_{DD} = 4.0 to 5.5 V	4/f_X		μs

Note fbr: set baud rate

(f) I²C bus Mode

Parameter		Symbol	Standard Mode		High-speed Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCL0 clock frequency		f_{CLK}	0	100	0	400	kHz
Bus free time (between stop and start condition)		t_{BUF}	4.7	—	1.3	—	μs
Hold time[Note 1]		$t_{HD:STA}$	4.0	—	0.6	—	μs
SCL0 clock low-level width		t_{LOW}	4.7	—	1.3	—	μs
SCL0 clock high-level width		t_{HIGH}	4.0	—	0.6	—	μs
Start/restart condition setup time		$t_{SU:STA}$	4.7	—	0.6	—	μs
Data hold time	CBUS compatible master	$t_{HD:DAT}$	5.0	—	—	—	μs
	I²C bus		0[Note 2]	—	0[Note 2]	0.9[Note 3]	μs
Data setup time		$t_{SU:DAT}$	250	—	100[Note 4]	—	ns
SDA0 and SCL0 signal rise time		t_R	—	1000	20 + 0.1Cb[Note 5]	300	ns
SDA0 and SCL0 signal fall time		t_F	—	300	20 + 0.1Cb[Note 5]	300	ns
Stop condition setup time		$t_{SU:STO}$	4.0	—	0.6	—	μs
Spike pulse width controlled by input filter		t_{SP}	—	—	0	50	ns
Capacitive load per each bus line		Cb	—	400	—	400	pF

Notes 1. In the start condition, the first clock pulse is generated after this hold time.

2. To fill in the undefined area of the SCL0 falling edge, it is necessary for the device to internally provide at least 300 ns of hold time for the SDA0 signal (which is $V_{IHmin.}$ of the SCL0 signal).

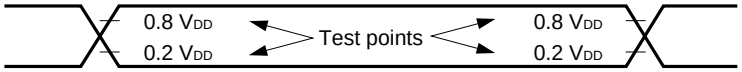
3. If the device does not extend the SCL0 signal low hold time (t_{LOW}), only maximum data hold time $t_{HD:DAT}$ needs to be fulfilled.

4. The high-speed mode I²C bus is available in a standard mode I²C bus system. At this time, the conditions described below must be satisfied.

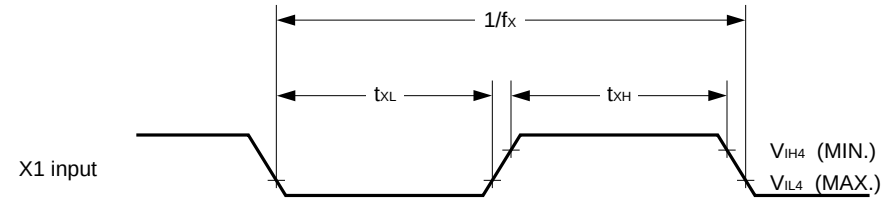
- If the device does not extend the SCL0 signal low state hold time
  $t_{SU:DAT} \geq 250$ ns
- If the device extends the SCL0 signal low state hold time
  Be sure to transmit the next data bit to the SDA0 line before the SCL0 line is released ($t_{Rmax.} + t_{SU:DAT}$ = 1000 + 250 = 1250 ns by standard mode I²C bus specification).

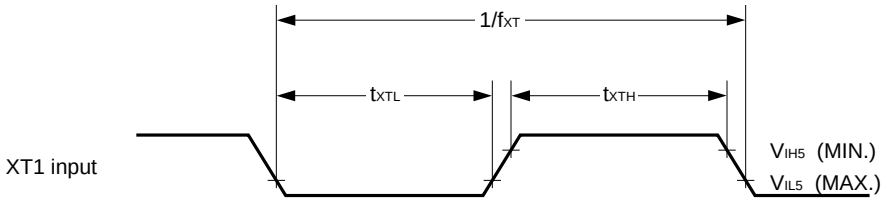
5. Cb: Total capacitance per one bus line (unit: pF)

AC Timing Test Point (Excluding X1, XT1 Input)

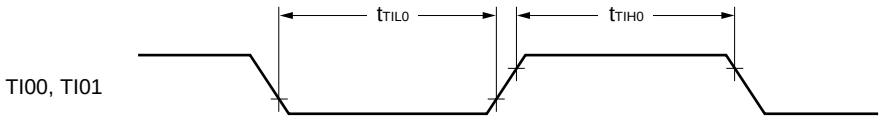


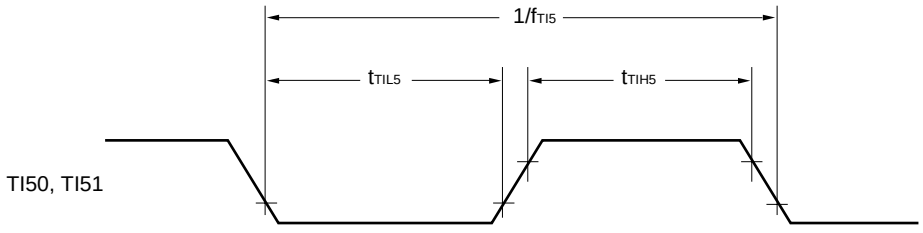
Clock Timing





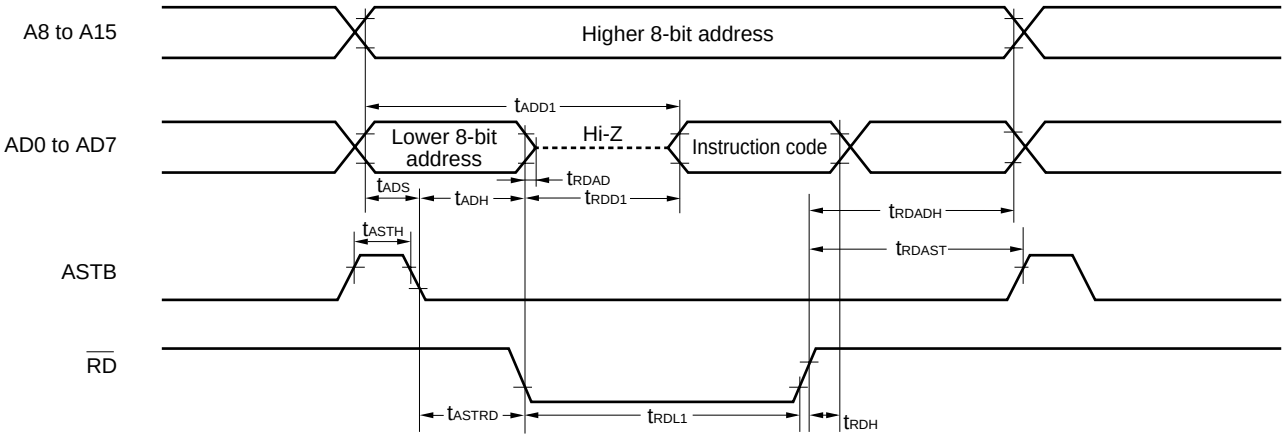
TI Timing



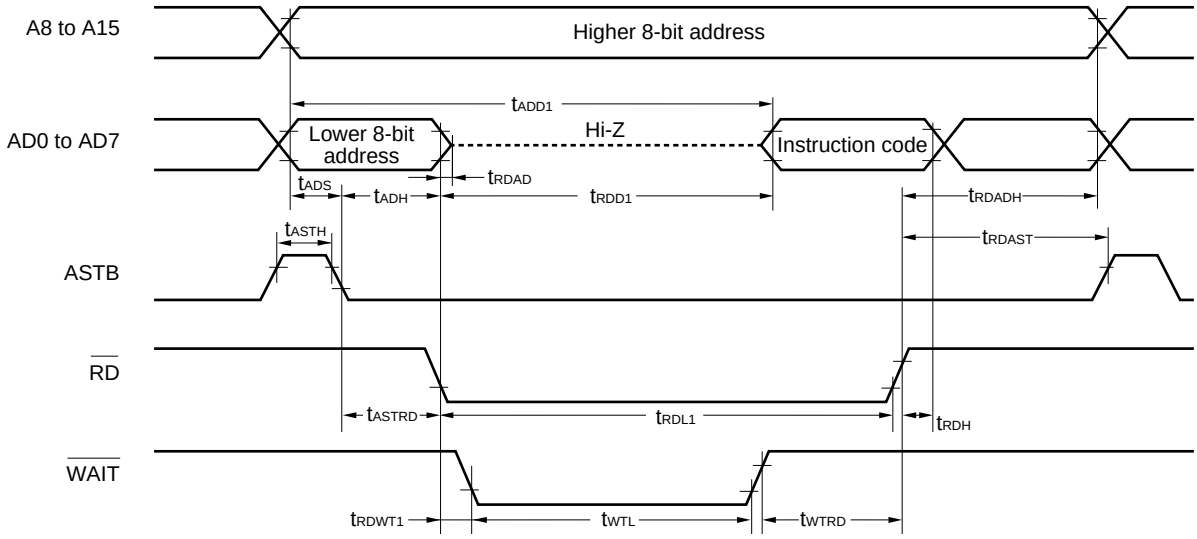


Read/Write Operation

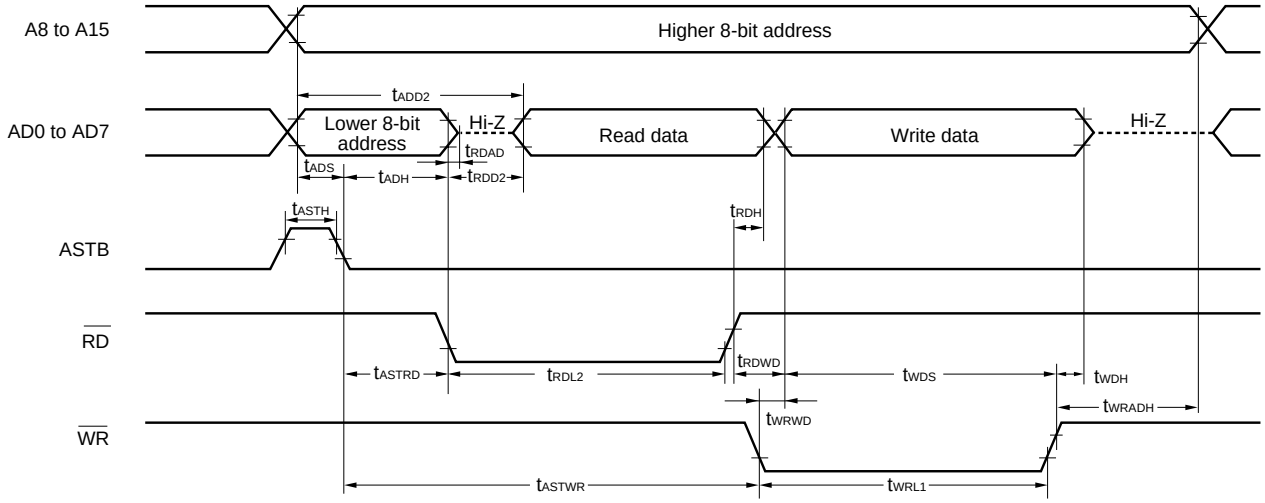
External Fetch (No Wait):



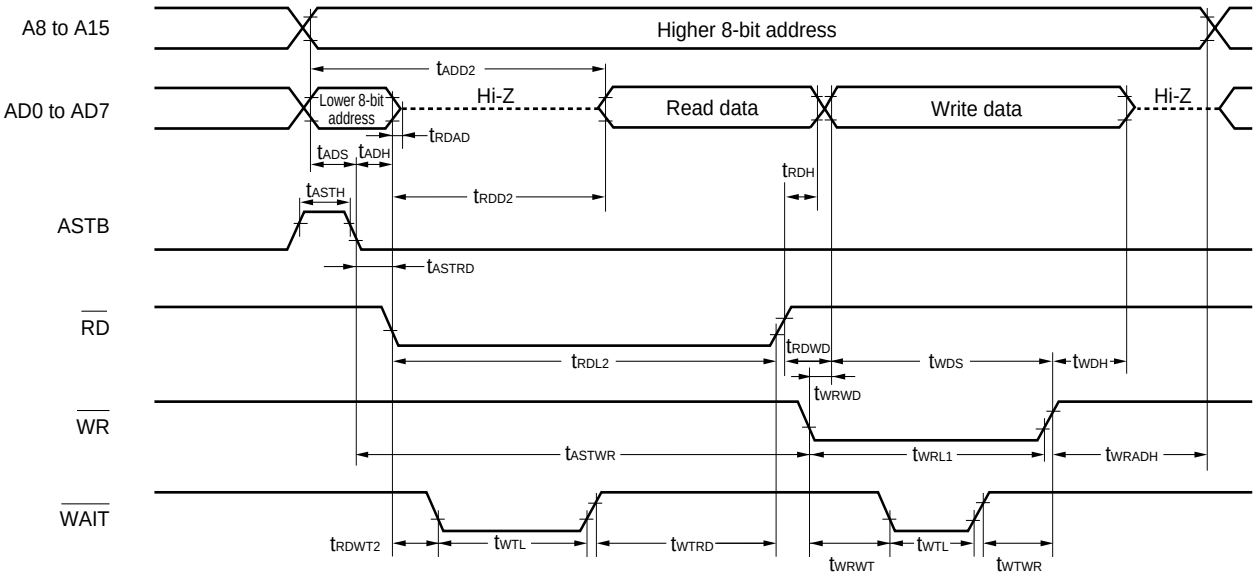
External Fetch (Wait Insertion):



External Data Access (No Wait):

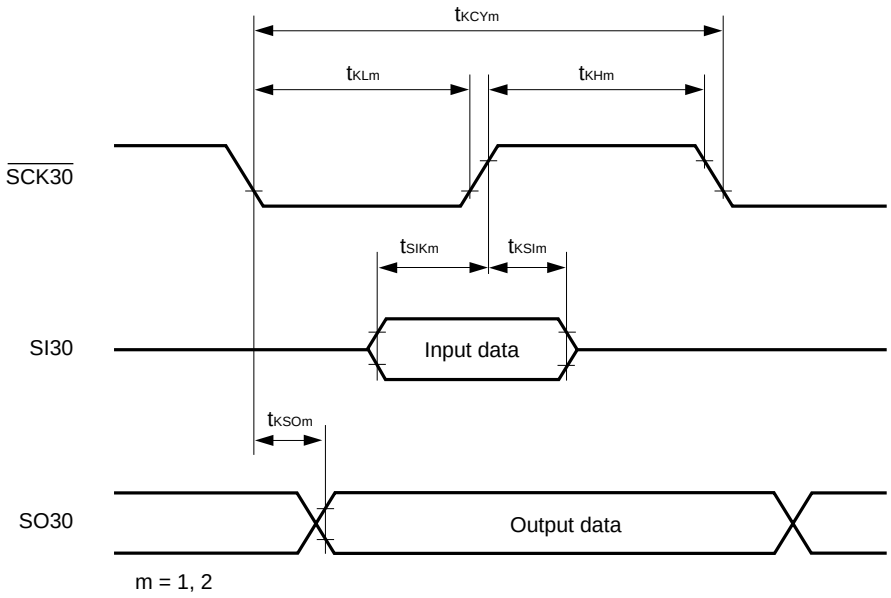


External Data Access (Wait Insertion):



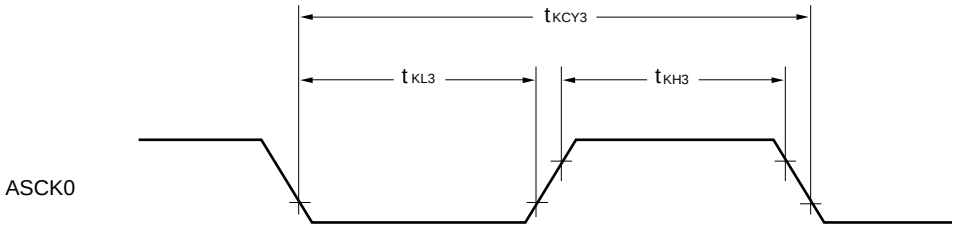
Serial Transfer Timing

3-Wire Serial I/O Mode:

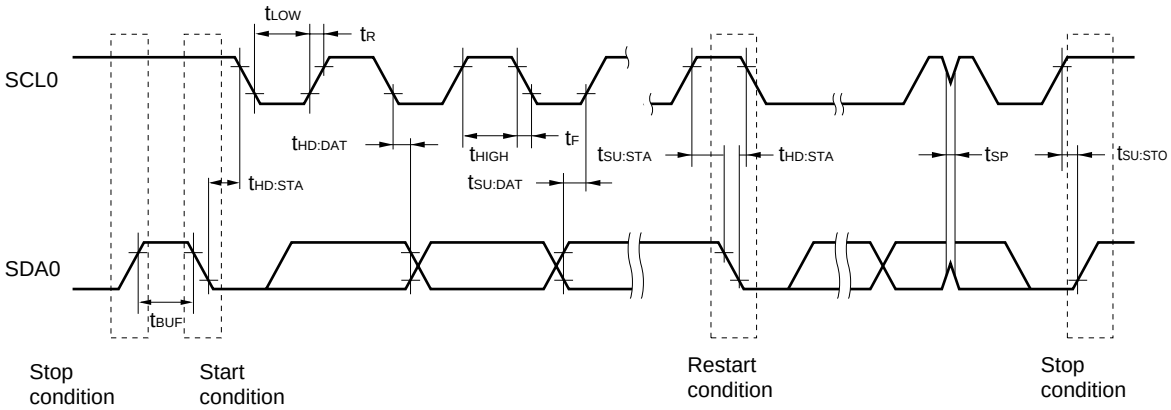


m = 1, 2

UART Mode (External Clock Input):



I²C Bus Mode:



A/D Converter Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = AV_{REF} = 1.8 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	bit
Overall error**Notes 1, 2**		4.0 V ≤ AV_{REF} ≤ 5.5 V		±0.2	±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V		±0.3	±0.6	%FSR
		1.8 V ≤ AV_{REF} < 2.7 V		±0.6	±1.2	%FSR
Conversion time	t_{CONV}	4.0 V ≤ AV_{REF} ≤ 5.5 V	14		96	μs
		2.7 V ≤ AV_{REF} < 4.0 V	19		96	μs
		1.8 V ≤ AV_{REF} < 2.7 V	28		96	μs
Zero-scale offset**Notes 1, 2**		4.0 V ≤ AV_{REF} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V			±0.6	%FSR
		1.8 V ≤ AV_{REF} < 2.7 V			±1.2	%FSR
Full-scale offset**Notes 1, 2**		4.0 V ≤ AV_{REF} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V			±0.6	%FSR
		1.8 V ≤ AV_{REF} < 2.7 V			±1.2	%FSR
Integral linearity error**Note 1**		4.0 V ≤ AV_{REF} ≤ 5.5 V			±2.5	LSB
		2.7 V ≤ AV_{REF} < 4.0 V			±4.5	LSB
		1.8 V ≤ AV_{REF} < 2.7 V			±8.5	LSB
Differential linearity error**Note 1**		4.0 V ≤ AV_{REF} ≤ 5.5 V			±1.5	LSB
		2.7 V ≤ AV_{REF} ≤ 4.0 V			±2.0	LSB
		1.8 V ≤ AV_{REF} < 2.7 V			±3.5	LSB
Analog input voltage	V_{IAN}		0		AV_{REF}	V
Reference voltage	AV_{REF}		1.8		AV_{DD}	V
Resistance between AV_{REF} and AV_{SS}	R_{REF}	A/D conversion is not performed	20	40		kΩ

Notes 1. Excluding quantization error (±1/2 LSB).

2. Shown as a percentage of the full scale value.

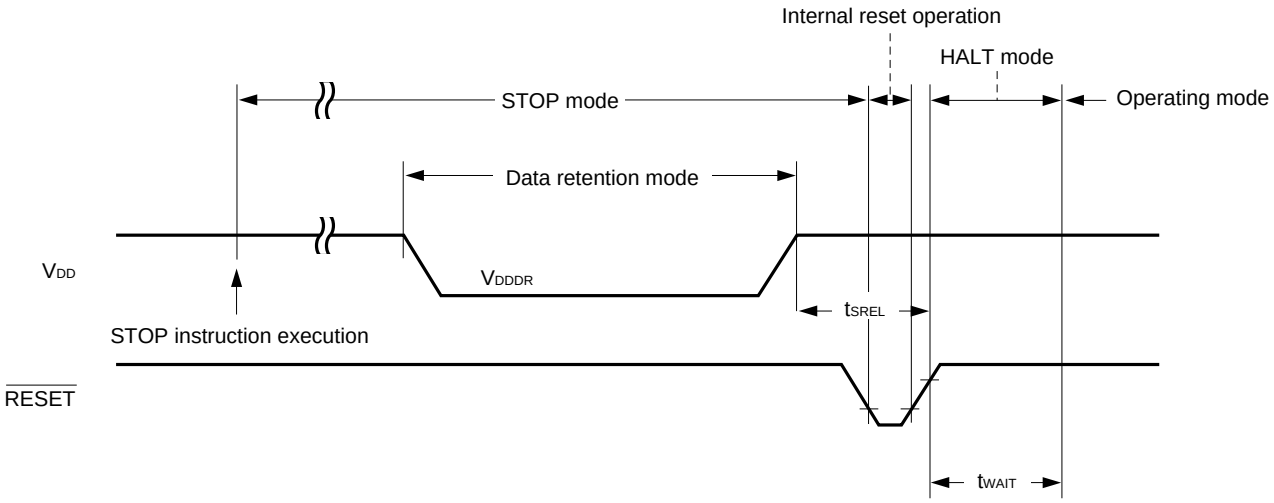
Remark When the μPD78F0034AY is used as an 8-bit resolution A/D converter, the specifications are the same as for the μPD780024AY Subseries A/D converter.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

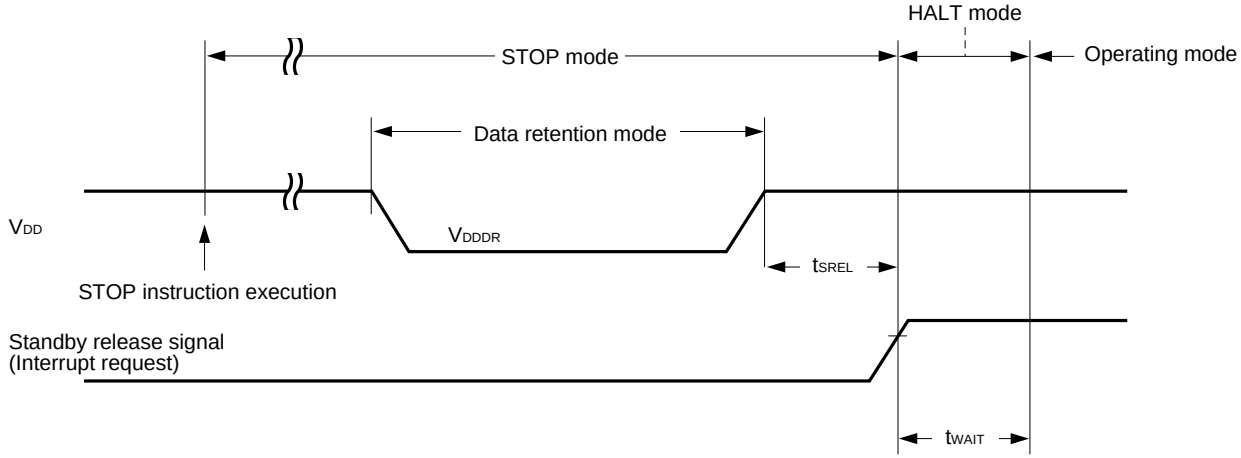
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.6		5.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 1.6 V Subsystem clock unassigned and feed-back resistor disconnected		0.1	30	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{\text{RESET}}$		$2^{17}/f_X$		ms
		Release by interrupt request		**Note**		ms

Note Selection of $2^{12}/f_X$ and $2^{14}/f_X$ to $2^{17}/f_X$ is possible using bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).

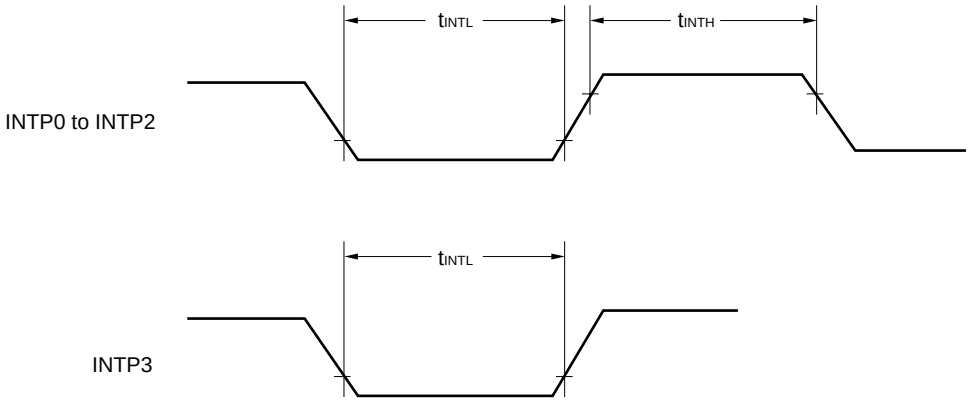
Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)



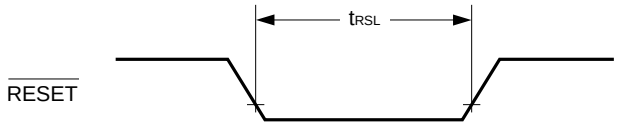
Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Request Signal)



Interrupt Request Input Timing



$\overline{\text{RESET}}$ Input Timing



Flash Memory Programming Characteristics (V_{DD} = 2.7 to 5.5 V, V_{SS} = 0 V, V_{PP} = 9.7 to 10.3 V)

(1) Basic characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating frequency	f_X	4.0 ≤ V_{DD} ≤ 5.5 V	1.0 Note 1		8.38	MHz
		2.7 ≤ V_{DD} < 4.0 V	1.0 Note 1		5.0	MHz
Supply voltage	V_{DD}	Operation voltage when writing	2.7		5.5	V
	V_{PPL}	Upon V_{PP} low-level detection	0		0.2 V_{DD}	V
	V_{PP}	Upon V_{PP} high-level detection	0.8 V_{DD}	V_{DD}	1.2 V_{DD}	V
	V_{PPH}	Upon V_{PP} high-voltage detection	9.7 Note 2	10.0 Note 2	10.3 Note 2	V
V_{DD} supply current	I_{DD}				10	mA
V_{PP} supply current	I_{PP}	V_{PP} =10.0 V		75	100	mA
Write time (per byte)	T_{WRT}		50		500	μs
Number of rewrites	C_{WRT}				20 Note 3	Times
Erase time	T_{ERASE}		1		20	s
Programming temperature	T_{PRG}		+10		+40	°C

Notes 1. When writing to flash memory by using I^2C bus, the operating frequency is 4.19 MHz (MIN.).

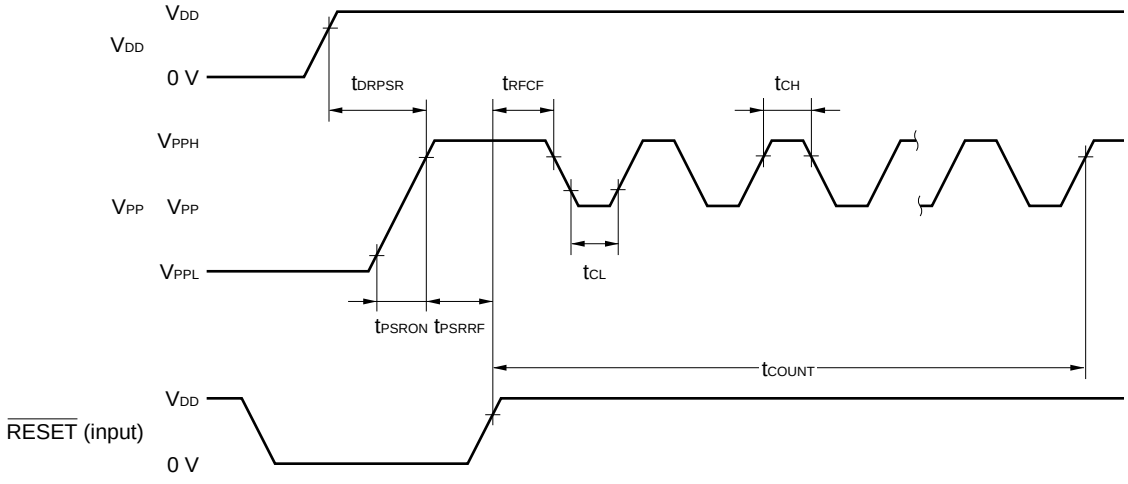
2. For the products specified as K, E, or P, 10.2 V (MIN.), 10.3 V (TYP.), and 10.4 V (MAX.) are applied.

3. For the products specified as K or E, the number is 1 (MAX.).

(2) Serial write operation characteristics

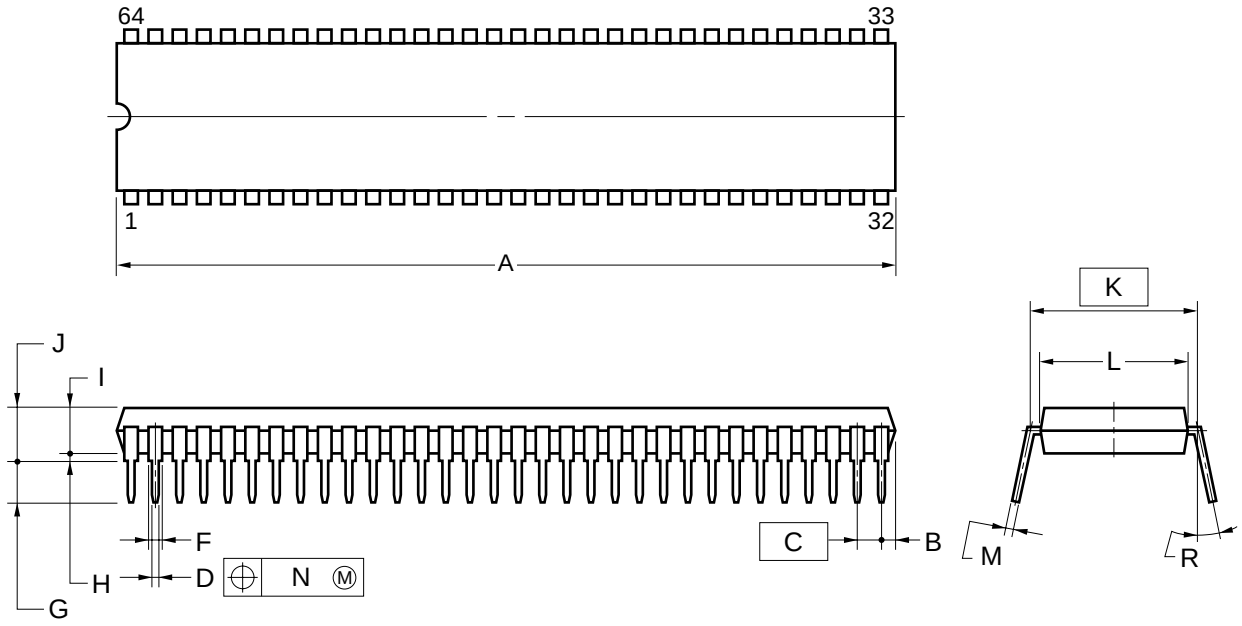
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{PP} set time	t_{PSRON}	V_{PP} high voltage	1.0			μs
V_{PP}↑ set time from V_{DD}↑	t_{DRPSR}	V_{PP} high voltage	1.0			μs
$\overline{RESET}$↑ set time from V_{PP}↑	t_{PSRRF}	V_{PP} high voltage	1.0			μs
V_{PP} count start time from $\overline{RESET}$↑	t_{RFCF}		1.0			μs
Count execution time	t_{COUNT}				2.0	ms
V_{PP} counter high-level width	t_{CH}		8.0			μs
V_{PP} counter low-level width	t_{CL}		8.0			μs
V_{PP} counter noise elimination width	t_{NFW}			40		ns

Flash Memory Write Mode Set Timing



6. PACKAGE DRAWINGS

64 PIN PLASTIC SHRINK DIP (750 mil)



NOTES

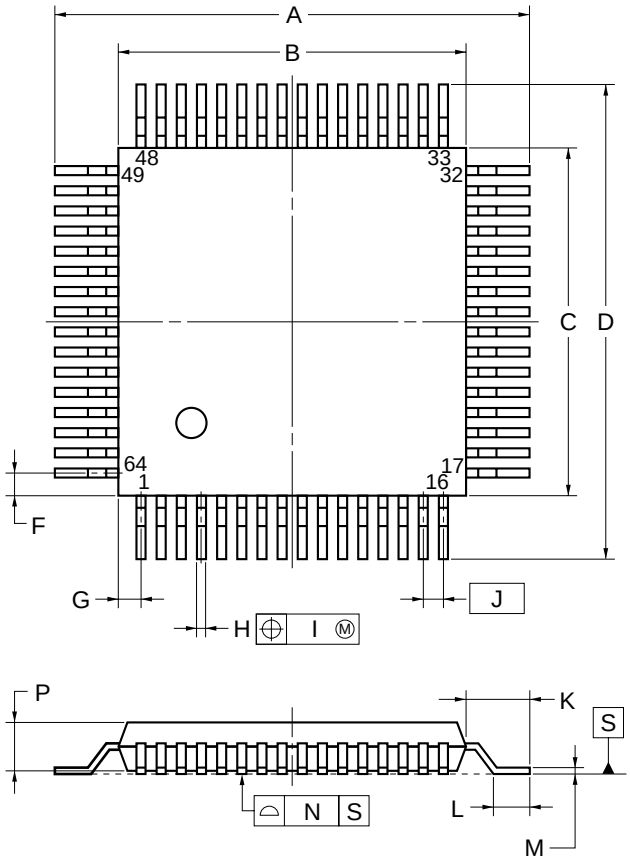
1. Controlling dimension—— millimeter.
2. Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
3. Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	$58.0^{+0.68}_{-0.20}$	$2.283^{+0.028}_{-0.008}$
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50±0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	$4.05^{+0.26}_{-0.20}$	$0.159^{+0.011}_{-0.008}$
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0±0.2	$0.669^{+0.009}_{-0.008}$
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0 to 15°	0 to 15°

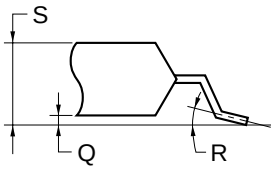
P64C-70-750A,C-3

Remark The package and material of ES products are the same as mass produced products.

64 PIN PLASTIC QFP (□14)



detail of lead end



NOTE

1. Controlling dimension —— millimeter.

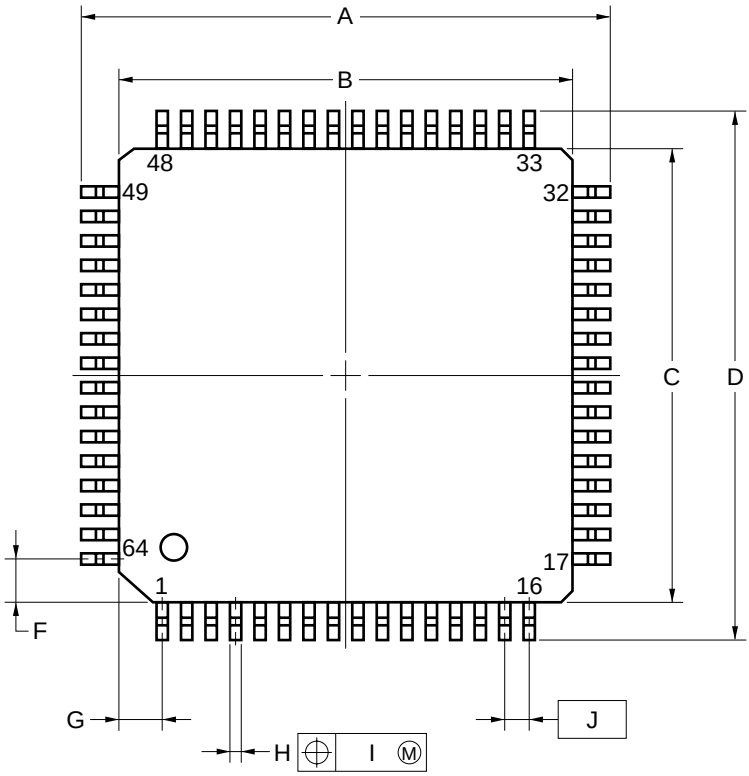
2. Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.6±0.4	0.693±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	$0.37^{+0.08}_{-0.07}$	$0.015^{+0.003}_{-0.004}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.17^{+0.08}_{-0.07}$	$0.007^{+0.003}_{-0.004}$
N	0.10	0.004
P	2.55±0.1	0.100±0.004
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	2.85 MAX.	0.113 MAX.

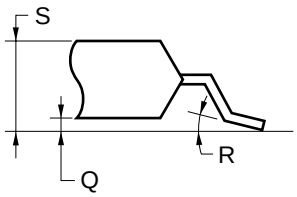
P64GC-80-AB8-4

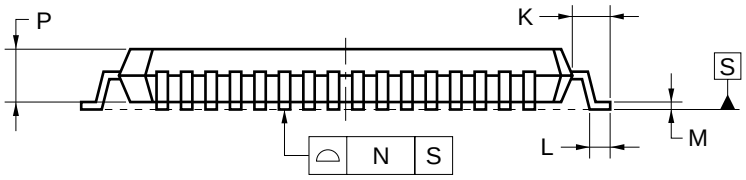
Remark The package and material of ES products are the same as mass produced products.

64 PIN PLASTIC LQFP (12x12)



detail of lead end





NOTES

1. Controlling dimension — millimeter.

2. Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	14.8±0.4	0.583±0.016
B	12.0±0.2	$0.472^{+0.009}_{-0.008}$
C	12.0±0.2	$0.472^{+0.009}_{-0.008}$
D	14.8±0.4	0.583±0.016
F	1.125	0.044
G	1.125	0.044
H	0.32±0.08	$0.013^{+0.003}_{-0.004}$
I	0.13	0.005
J	0.65 (T.P.)	0.026
K	1.4±0.2	0.055±0.008
L	0.6±0.2	$0.024^{+0.008}_{-0.009}$
M	$0.17^{+0.08}_{-0.07}$	$0.007^{+0.003}_{-0.004}$
N	0.10	0.004
P	1.4±0.1	$0.055^{+0.004}_{-0.005}$
Q	0.125±0.075	0.005±0.003
R	5°±5°	5°±5°
S	1.7 MAX.	0.067 MAX.

P64GK-65-8A8-2

Remark The package and material of ES products are the same as mass produced products.

7. RECOMMENDED SOLDERING CONDITIONS

The μPD78F0034AY should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Table 7-1. Surface Mounting Type Soldering Conditions

(1) μPD78F0034AYGC-AB8: 64-pin plastic QFP (14 × 14 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds Max. (at 210°C or higher), Count: Two times or less	IR35-00-2
VPS	Package peak temperature: 215°C, Time: 40 seconds Max. (at 200°C or higher), Count: Two times or less	VP15-00-2
Wave soldering	Solder bath temperature: 260°C Max., Time: 10 seconds Max., Count: Once, Preheating temperature: 120°C Max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C Max., Time: 3 seconds Max. (per pin row)	–

Caution Do not use different soldering methods together (except for partial heating).

(2) μPD78F0034AYGK-8A8: 64-pin plastic LQFP (12 × 12 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds Max. (at 210°C or higher), Count: Two times or less, Exposure limit: 7 days[Note] (after 7 days, prebake at 125°C for 10 hours)	IR35-107-2
VPS	Package peak temperature: 215°C, Time: 40 seconds Max. (at 200°C or higher), Count: Two times or less, Exposure limit: 7 days[Note] (after 7 days, prebake at 125°C for 10 hours)	VP15-107-2
Wave soldering	Solder bath temperature: 260°C Max., Time: 10 seconds Max., Count: Once, Preheating temperature: 120°C Max. (package surface temperature) Exposure limit: 7 days[Note] (after 7 days, prebake at 125°C for 10 hours)	WS60-107-1
Partial heating	Pin temperature: 300°C Max., Time: 3 seconds Max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

Table 7-2. Through-Hole Type Soldering Conditions

μPD78F0034AYCW: 64-pin plastic shrink DIP (750 mils)

Soldering Method	Soldering Conditions
Wave soldering (pin only)	Solder bath temperature: 260°C Max., Time: 10 seconds Max.
Partial heating	Pin temperature: 300°C Max., Time: 3 seconds Max. (per pin row)

Caution Apply wave soldering only to the pins and be careful not to bring solder into direct contact with the package.

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD78F0034AY Subseries. Also refer to **(5) Cautions on Using Development Tools**.

(1) Language Processing Software

RA78K/0	Assembler package common to 78K/0 Series
CC78K/0	C compiler package common to 78K/0 Series
DF780034	Device file common to μPD780034A Subseries
CC78K/0-L	C compiler library source file common to 78K/0 Series

(2) Flash Memory Writing Tools

Flashpro II (type No. FL-PR2), Flashpro III (type No. FL-PR3, PG-FP3)	Flash programmer dedicated to microcontrollers with on-chip flash memory
FA-64CW, FA-64GC, FA-64GK	Adapter for flash memory writing

(3) Debugging Tools

When IE-78K0-NS in-circuit emulator is used

IE-78K0-NS	In-circuit emulator common to 78K/0 Series
IE-70000-MC-PS-B	Power supply unit for IE-78K0-NS
IE-78K0-NS-PA**Note**	Performance board that enhances and expands the IE-78K0-NS functions
IE-70000-98-IF-C	Interface adapter used when PD-9800 Series PC (except notebook type) is used as host machine (C bus supported)
IE-70000-CD-IF-A	PC card and interface cable when PC-9800 Series notebook PC is used as host machine (PCMCIA socket supported)
IE-70000-PC-IF-C	Interface adapter when using IBM PC/AT™ or compatible as host machine (ISA bus supported)
IE-70000-PCI-IF	Adapter necessary when using PCI-bus incorporated personal computer as host machine
IE-780034-NS-EM1	Emulation board to emulate the μPD780034AY Subseries
NP-64CW	Emulation probe for 64-pin plastic shrink DIP (CW type)
NP-64GC	Emulation probe for 64-pin plastic QFP (CG-AB8 type)
NP-64GK	Emulation probe for 64-pin plastic LQFP (CG-8A8 type)
TGK-064SBW	Conversion adapter to connect the NP-64GK and a target system board on which the 64-pin plastic LQFP (GC-8A8 type) can be mounted
EV-9200GC-64	Socket mounted on target system board for the 64-pin plastic QFP (GC-AB8 type)
ID78K0-NS	Integrated debugger for IE-78K0-NS
SM78K0	System simulator common to 78K/0 Series
DF780034	Device file common to μPD780034A Subseries

Note Under development

When using in-circuit emulator IE-78001-R-A

IE-78001-R-A	In-circuit emulator common to 78K/0 Series
IE-70000-98-IF-C	Interface adapter when using PC-9800 series as host machine (excluding notebook PCs) (C bus supported)
IE-70000-PC-IF-C	Interface adapter when using IBM PC/AT or compatible as host machine (ISA bus supported)
IE-70000-PCI-IF	Adapter necessary when using PCI-bus incorporated personal computers as host machine.
IE-78000-R-SV3	Interface adapter and cable when using EWS as host machine
IE-780034-NS-EM1	Emulation board to emulate μPD780034AY Subseries
IE-78K0-R-EX1	Emulation probe conversion board to use IE-780034-NS-EM1 on IE-78001-R-A
EP-78240CW-R	Emulation probe for 64-pin plastic shrink DIP (CW type)
EP-78240GC-R	Emulation probe for 64-pin plastic QFP (GC-AB8 type)
EP-78012GK-R	Emulation probe for 64-pin plastic LQFP (GK-8A8 type)
TGK-064SBW	Conversion adapter for connecting target system board designed to allow mounting of 64-pin plastic LQFP (GK-8A8) and NP-64GK.
EV-9200GC-64	Socket to be mounted on target system board manufactured for 64-pin plastic QFP (GC-AB8 type)
ID78K0	Integrated debugger for IE-78001-R-A
SM78K0	System simulator common to 78K/0 Series
DF780034	Device file common to μPD780034A Subseries

(4) Real-time OS

RX78K/0	Real-time OS for 78K/0 Series
MX78K0	OS for 78K/0 Series

(5) Cautions on using development tools

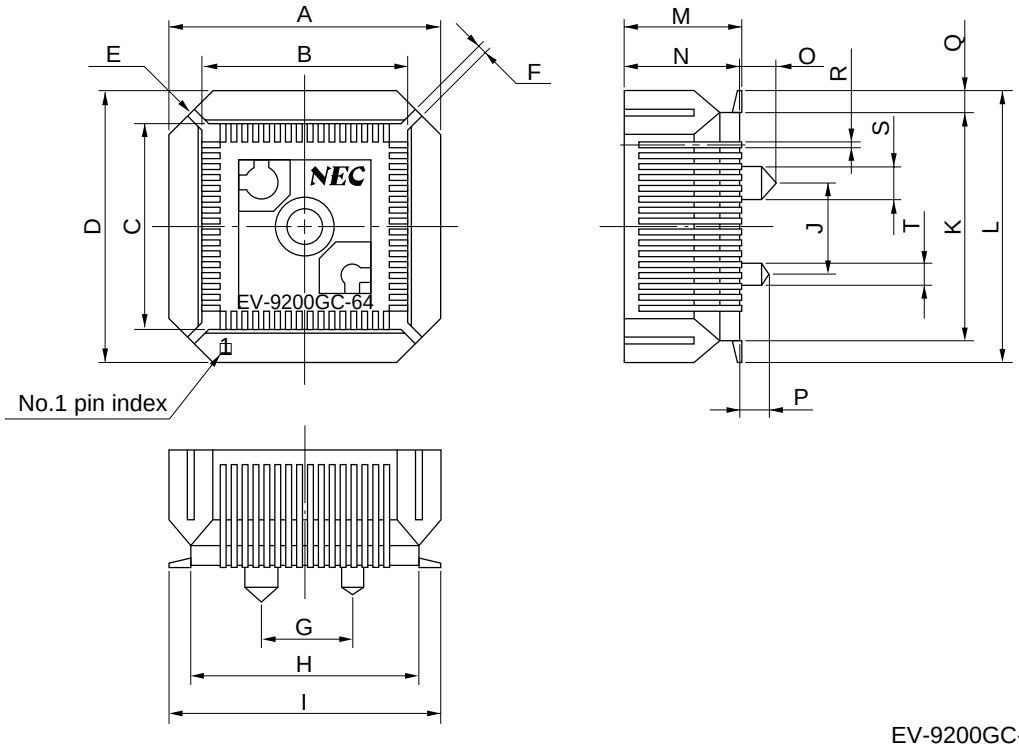
- The ID-78K0-NS, ID78K0, and SM78K0 are used in combination with the DF780034.
- The CC78K/0 and RX78K/0 are used in combination with the RA78K/0 and the DF780034.
- The FL-PR2, FL-PR3, FA-64CW, FA-64GC, FA64GK, NP-64CW, NP64GC, and NP-64GK are products made by Naito Densei Machida Mfg. Co., Ltd. (+81-44-822-3813).
  Contact an NEC distributor regarding the purchase of these products.
- The TGK-064SBW is a product made by TOKYO ELETECH CORPORATION.
  For further information contact Daimaru Kogyo, Ltd.
  Tokyo Electronic Division (+81-3-3820-7112)
  Osaka Electronic Division (+81-6-6244-6672)
- For third party development tools, see the **78K/0 Series Selection Guide (U11126E)**.
- The host machines and OSs supporting each software are as follows.

Host Machine / [OS] / Software	PC PC-9800 series [Windows™] IBM PC/AT or compatibles [Japanese/English Windows]	EWS HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™, Solaris™] NEWS™ (RISC) [NEWS-OS™]
RA78K/0	√**Note**	√
CC78K/0	√**Note**	√
ID78K0-NS	√	–
ID78K0	√	√
SM78K0	√	–
RX78K/0	√**Note**	√
MX78K0	√**Note**	√

Note DOS-based software

Conversion Socket Drawing (EV-9200GC-64) and Footprints

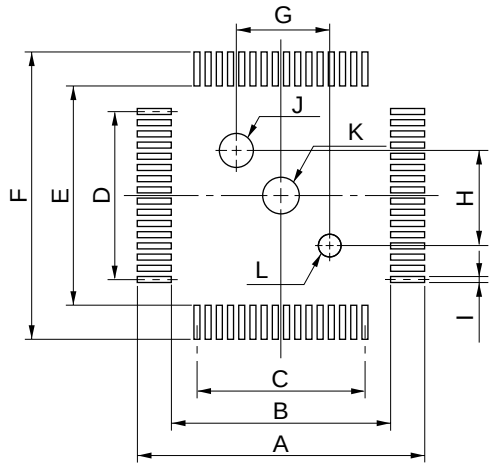
Figure A-1. EV-9200GC-64 Drawing (For Reference Only)



EV-9200GC-64-G0

ITEM	MILLIMETERS	INCHES
A	18.8	0.74
B	14.1	0.555
C	14.1	0.555
D	18.8	0.74
E	4-C 3.0	4-C 0.118
F	0.8	0.031
G	6.0	0.236
H	15.8	0.622
I	18.5	0.728
J	6.0	0.236
K	15.8	0.622
L	18.5	0.728
M	8.0	0.315
N	7.8	0.307
O	2.5	0.098
P	2.0	0.079
Q	1.35	0.053
R	0.35±0.1	$0.014^{+0.004}_{-0.005}$
S	φ2.3	φ0.091
T	φ1.5	φ0.059

Figure A-2. EV-9200GC-64 Footprints (For Reference Only)



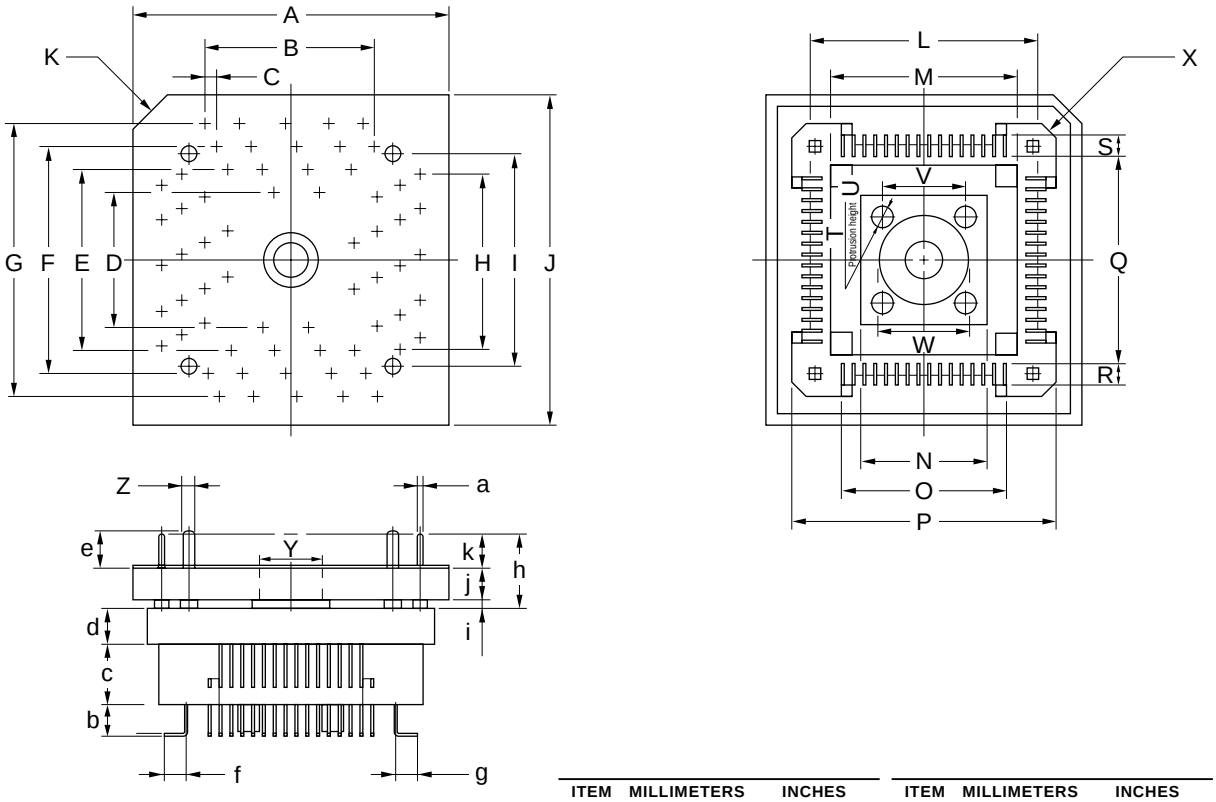
EV-9200GC-64-P1E

ITEM	MILLIMETERS	INCHES
A	19.5	0.768
B	14.8	0.583
C	$0.8\pm0.02\times15=12.0\pm0.05$	$0.031^{+0.002}_{-0.001}\times0.591=0.472^{+0.003}_{-0.002}$
D	$0.8\pm0.02\times15=12.0\pm0.05$	$0.031^{+0.002}_{-0.001}\times0.591=0.472^{+0.003}_{-0.002}$
E	14.8	0.583
F	19.5	0.768
G	6.00 ± 0.08	$0.236^{+0.004}_{-0.003}$
H	6.00 ± 0.08	$0.236^{+0.004}_{-0.003}$
I	0.5 ± 0.02	$0.197^{+0.001}_{-0.002}$
J	$\phi2.36\pm0.03$	$\phi0.093^{+0.001}_{-0.002}$
K	$\phi2.2\pm0.1$	$\phi0.087^{+0.004}_{-0.005}$
L	$\phi1.57\pm0.03$	$\phi0.062^{+0.001}_{-0.002}$

Caution Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E).

Conversion Adapter Drawing (TGK-064SBW)

Figure A-3. TGK-064SBW Drawing (For Reference Only)



ITEM	MILLIMETERS	INCHES
A	18.4	0.724
B	0.65x15=9.75	0.026x0.591=0.384
C	0.65	0.026
D	7.75	0.305
E	10.15	0.400
F	12.55	0.494
G	14.95	0.589
H	0.65x15=9.75	0.026x0.591=0.384
I	11.85	0.467
J	18.4	0.724
K	C 2.0	C 0.079
L	12.45	0.490
M	10.25	0.404
N	7.7	0.303
O	10.02	0.394
P	14.92	0.587
Q	11.1	0.437
R	1.45	0.057
S	1.45	0.057
T	4-ϕ1.3	4-ϕ0.051
U	1.8	0.071
V	5.0	0.197
W	ϕ5.3	ϕ0.209
X	4-C 1.0	4-C 0.039
Y	ϕ3.55	ϕ0.140
Z	ϕ0.9	ϕ0.035

ITEM	MILLIMETERS	INCHES
a	ϕ0.3	ϕ0.012
b	1.85	0.073
c	3.5	0.138
d	2.0	0.079
e	3.9	0.154
f	1.325	0.052
g	1.325	0.052
h	5.9	0.232
i	0.8	0.031
j	2.4	0.094
k	2.7	0.106

TGK-064SBW-G0E

Note: Product made by TOKYO ELETECH CORPORATION.

APPENDIX B. RELATED DOCUMENTS

Device Related Documents

Document Name	Document No. (English)	Document No. (Japanese)
μPD780024A, 780034A, 780024AY, 780034AY Subseries User's Manual	U14046E	U14046J
μPD780031AY, 780032AY, 780033AY, 780034AY Data Sheet	U14043E	U14043J
μPD78F0034AY Data Sheet	This manual	U14041J
78K/0 Series User's Manual Instruction	U12326E	U12326J
78K/0 Series Instruction Table	—	U10903J
78K/0 Series Instruction Set	—	U10904J

Development Tool Documents (User's Manuals)

Document Name		Document No. (English)	Document No. (Japanese)
RA78K0 Assembler Package	Operation	U11802E	U11802J
	Assembly Language	U11801E	U11801J
	Structured Assembly Language	U11789E	U11789J
RA78K Series Structured Assembler Preprocessor		EEU-1402	U12323J
CC78K/0 C Compiler	Operation	U11517E	U11517J
	Language	U11518E	U11518J
CC78K/0 C Compiler Application Note	Programming Know-how	U13034E	U13034J
IE-78K0-NS		To be prepared	To be prepared
IE-78001-R-A		To be prepared	To be prepared
IE-780034-NS-EM1		To be prepared	To be prepared
EP-78240		U10332E	EEU-986
EP-78012GK-R		EEU-1538	EEU-5012
SM78K0 System Simulator-Windows based	Reference	U10181E	U10181J
SM78K Series System Simulator	External Part User Open Interface Specifications	U10092E	U10092J
ID78K0-NS Integrated Debugger Windows based	Reference	U12900E	U12900J
ID78K0 Integrated Debugger EWS based	Reference	—	U11151J
ID78K0 Integrated Debugger PC based	Reference	U11539E	U11539J
ID78K0 Integrated Debugger Windows based	Guide	U11649E	U11649J

Caution The above related documents are subject to change without notice. Be sure to read the latest documents before designing.

Embedded Software Documents (User's Manuals)

Document Name		Document No. (English)	Document No. (Japanese)
78K/0 Series Real-time OS	Fundamental	U11537E	U11537J
	Installation	U11536E	U11536J
78K/0 Series OS MX78K0	Fundamental	U12257E	U12257J

Other Documents

Document Name	Document No. (English)	Document No. (Japanese)
SEMICONDUCTORS SELECTION GUIDE Products & Packages (CD-ROM)	X13769X	
Semiconductor Device Mounting Technology Manual	C10535E	C10535J
Quality Grades on NEC Semiconductor Devices	C11531E	C11531J
NEC Semiconductor Device Reliability/Quality Control System	C10983E	C10983J
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E	C11892J
Guide to Microcomputer - Related Products by Third Party		— U11416J

Caution The above related documents are subject to change without notice. Be sure to read the latest documents before designing.

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Purchase of NEC I^2C components conveys a license under the Philips I^2C patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Philips.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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