NEC

MOS INTEGRATED CIRCUIT

μPD78F0078, 78F0078Y

8-BIT SINGLE-CHIP MICROCONTROLLERS

DESCRIPTION

The μPD78F0078 is a product of the μPD780078 Subseries in the 78K/0 Series, and equivalent to the μPD780078 with a flash memory in place of internal ROM.

The μPD78F0078Y is a product of the μPD780078Y Subseries in the 78K/0 Series, and equivalent to the μPD780078Y with a flash memory in place of internal ROM.

This device can be programmed without being removed from the substrate.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD780076, 780078, 780076Y, 780078Y Subseries User's Manual : U14260E (On preparation)
78K/0 Series User's Manual – Instructions : U12326E

FEATURES

- Pin-compatible with mask ROM versions (except V_{PP} and HS pins)
- Flash memory: 60 Kbytes (self-programming compatible)
- Internal high-speed RAM: 1024 bytes
- Internal expansion RAM: 1024 bytes
- Supply voltage: V_{DD} = 2.7 to 5.5 V

Remark For the difference between the flash memory version and the mask ROM version, refer to **4. DIFFERENCES BETWEEN μPD78F0078, 78F0078Y AND MASK ROM VERSION.**

APPLICATIONS

Personal computers, air conditioners, dash boards, air bags, car audios, etc.

ORDERING INFORMATION

Part Number	Package
μPD78F0078GC-×××-AB8	64-pin plastic QFP (14 × 14 mm)
μPD78F0078GK-×××-8A8	64-pin plastic LQFP (12 × 12 mm)
μPD78F0078YGC-×××-AB8	64-pin plastic QFP (14 × 14 mm)
μPD78F0078YGK-×××-8A8	64-pin plastic LQFP (12 × 12 mm)

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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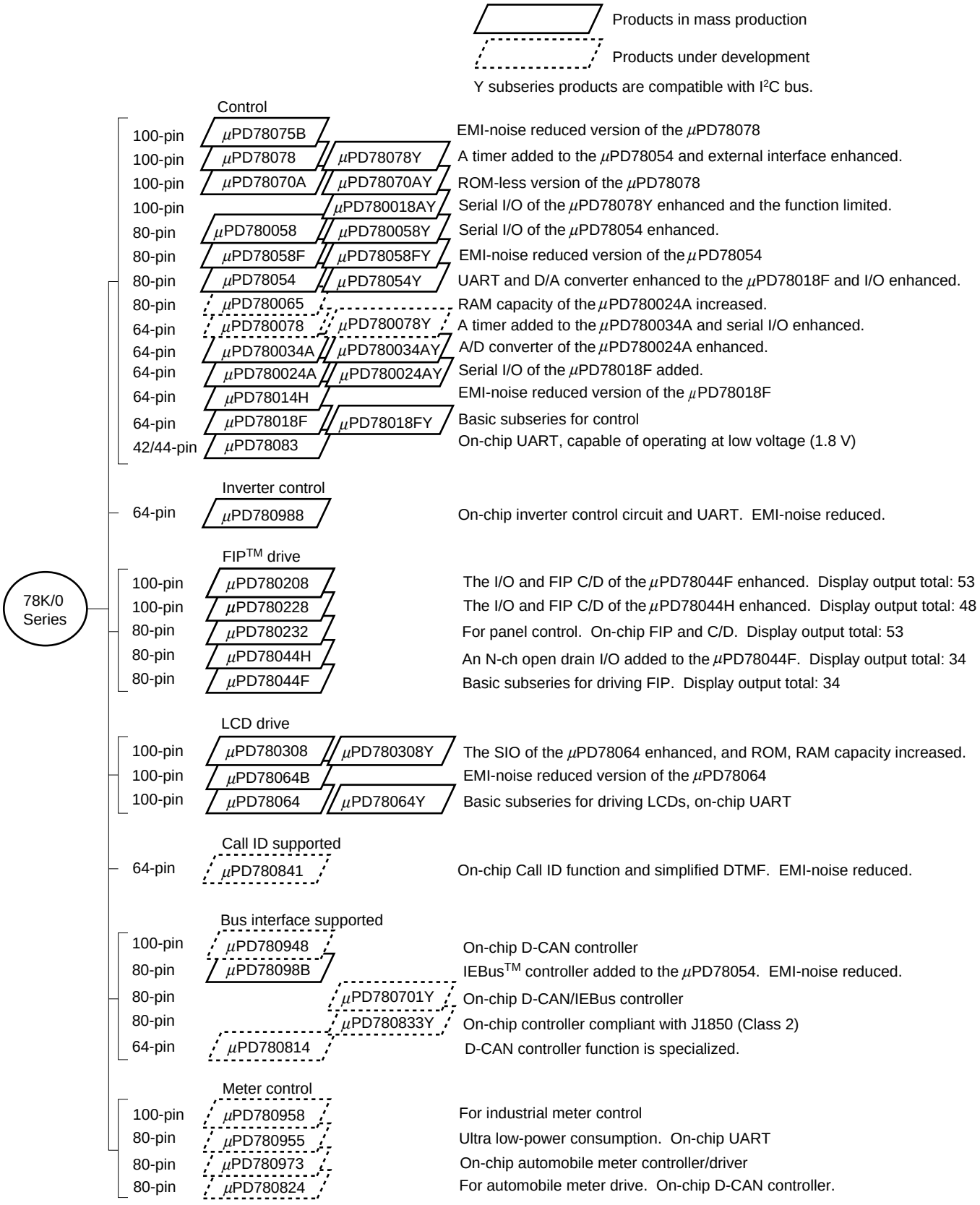
78K/0 SERIES DEVELOPMENT

The products in the 78K/0 series are listed below. The names enclosed in boxes are subseries names.



The major functional differences among the subseries are shown below.

Subseries Name \ Function		ROM Capacity	Timer 8-bit	Timer 16-bit	Timer Watch	Timer WDT	8-bit A/D	10-bit A/D	8-bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
Control	μPD78075B	32 K-40 K	4ch	1ch	1ch	1ch	8ch	–	2ch	3ch (UART: 1 ch)	88	1.8 V	Yes
	μPD78078	48 K-60 K											
	μPD78070A	–									61	2.7 V	
	μPD780058	24 K-60 K	2ch							3ch (time-division UART: 1ch)	68	1.8 V	
	μPD78058F	48 K-60 K								3ch (UART: 1ch)	69	2.7 V	
	μPD78054	16 K-60 K										2.0 V	
	μPD780065	40 K-48 K							–	4ch (UART: 1 ch)	60	2.7 V	
	μPD780078	48 K-60 K		2ch			–	8ch		3ch (UART: 2ch)	52	1.8 V	
	μPD780034A	8 K-32 K		1ch						3ch (UART: 1ch)	51		
	μPD780024A						8ch	–					
	μPD78014H									2ch	53		
	μPD78018F	8 K-60 K											
	μPD78083	8 K-16 K		–	–					1ch (UART: 1ch)	33		–
Inverter control	μPD780988	16 K-60 K	3ch	**Note**	–	1ch	–	8ch	–	3ch (UART: 2ch)	47	4.0 V	Yes
FIP drive	μPD780208	32 K-60 K	2ch	1ch	1ch	1ch	8ch	–	–	2ch	74	2.7 V	–
	μPD780228	48 K-60 K	3ch	–	–					1ch	72	4.5 V	
	μPD780232	16 K-24 K					4ch			2ch	40		
	μPD78044H	32 K-48 K	2ch	1ch	1ch		8ch			1ch	68	2.7 V	
	μPD78044F	16 K-40 K								2ch			
LCD drive	μPD780308	48 K-60 K	2ch	1ch	1ch	1ch	8ch	–	–	3ch (time-division UART: 1ch)	57	2.0 V	–
	μPD78064B	32 K								2ch (UART: 1ch)			
	μPD78064	16 K-32 K											
Call ID supported	μPD780841	24 K-32 K	2ch	–	1ch	1ch	2ch	–	–	2ch (UART: 1ch)	61	2.7 V	–
Bus interface supported	μPD780948	60 K	2ch	2ch	1ch	1ch	8ch	–	–	3ch (UART: 1ch)	79	4.0 V	Yes
	μPD78098B	40 K-60 K		1ch					2ch		69	2.7 V	–
	μPD780814	32 K-60 K		2ch			12ch		–	2ch (UART: 1ch)	46	4.0 V	
Meter control	μPD780958	48 K-60 K	4ch	2ch	–	1ch	–	–	–	2ch (UART: 1ch)	69	2.2 V	–
	μPD780955	40 K	6ch	1ch			1ch			2ch (UART: 2ch)	50		
	μPD780973	24 K-32 K	3ch		1ch		5ch			2ch (UART: 1ch)	56	4.5 V	
	μPD780824	32 K-60 K									59	4.0 V	

Note 16-bit timer: 2 channels
10-bit timer: 1 channel

The major functional differences among the Y subseries are shown below.

Subseries Name \ Function		ROM Capacity	Configuration of Serial Interface	I/O	V_{DD} MIN. Value
Control	μPD78078Y	48 K to 60 K	3-wire/2-wire/I^2C : 1 ch 3-wire with automatic transmit/receive function : 1 ch 3-wire/UART : 1 ch	88	1.8 V
	μPD78070A	–		61	2.7 V
	μPD780018AY	48 K to 60 K	3-wire with automatic transmit/receive function : 1 ch Time-division 3-wire : 1 ch I^2C bus (multimaster supported) : 1 ch	88	
	μPD780058Y	24 K to 60 K	3-wire/2-wire/I^2C : 1 ch 3-wire with automatic transmit/receive function : 1 ch 3-wire/time-division UART : 1 ch	68	1.8 V
	μPD78058FY	48 K to 60 K	3-wire/2-wire/I^2C : 1 ch 3-wire with automatic transmit/receive function : 1 ch 3-wire/UART : 1 ch	69	2.7 V
	μPD78054Y	16 K to 60 K			2.0 V
	μPD780078Y	48 K to 60 K	3-wire : 1 ch UART : 1 ch 3-wire/UART : 1 ch I^2C bus (multimaster supported) : 1 ch	52	1.8 V
	μPD780034AY	8 K to 32 K	UART : 1 ch 3-wire : 1 ch I^2C bus (multimaster supported) : 1 ch	51	1.8 V
	μPD780024AY				
	μPD78018FY	8 K to 60 K	3-wire/2-wire/I^2C : 1 ch 3-wire with automatic transmit/receive function : 1 ch	53	
LCD drive	μPD780308Y	48 K to 60 K	3-wire/2-wire/I^2C : 1 ch 3-wire/time-division UART : 1 ch 3-wire : 1 ch	57	2.0 V
	μPD78064Y	16 K to 32 K	3-wire/2-wire/I^2C : 1 ch 3-wire/UART : 1 ch		

Remark The functions other than the serial interface are common to the Subseries without Y.

FUNCTION OVERVIEW

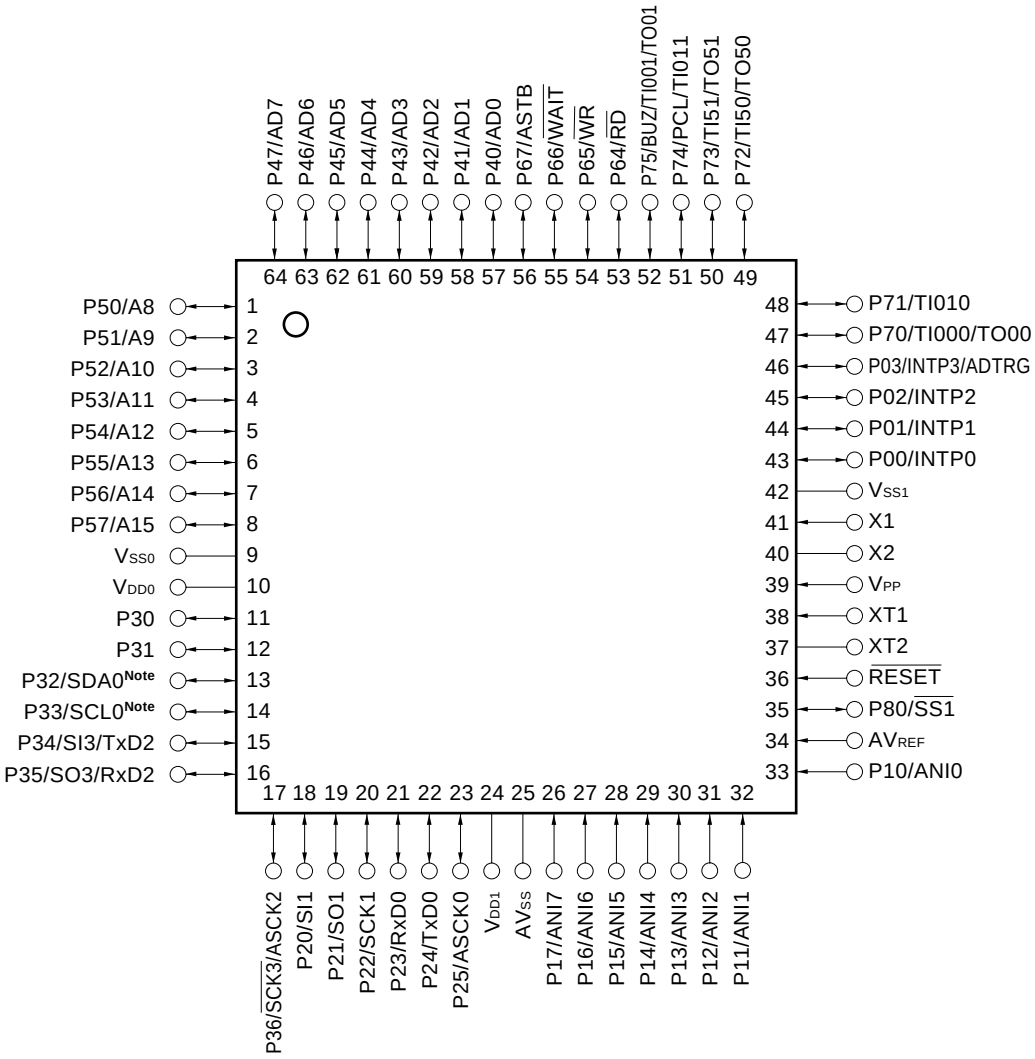
Item		μPD78F0078	μPD78F0078Y
Internal memory	Flash memory	60 Kbytes	
	High-speed RAM	1024 bytes	
	Expansion RAM	1024 bytes	
Memory space		64 Kbytes	
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)	
Minimum instruction execution time		On-chip variable function of minimum instruction execution time	
	When main system clock selected	0.24 μs/0.48 μs/0.95 μs/1.91 μs/3.81 μs (at 8.38-MHz operation)	
	When subsystem clock selected	122 μs (at 32.768-kHz operation)	
Instruction set		• 16-bit operation • Multiply/divide (8 bits × 8 bits,16 bits ÷ 8 bits) • Bit manipulate (set, reset, test, Boolean operation) • BCD adjust, etc.	
I/O ports		Total : 52 • CMOS input : 8 • CMOS I/O : 40 • N-ch open-drain I/O : 4	
A/D converter		• 10-bit resolution × 8 channels • Low-voltage operation available: AV_{DD} = 2.7 to 5.5 V	
Serial interface		• 3-wire serial I/O mode : 1 channel • UART mode : 1 channel • 3-wire serial I/O/UART mode selectable[Note] : 1 channel	• 3-wire serial I/O mode : 1 channel • UART mode : 1 channel • 3-wire serial I/O/UART mode selectable[Note] : 1 channel • I^2C bus mode : 1 channel
Timer		• 16-bit timer/event counter : 2 channels • 8-bit timer/event counter : 2 channels • Watch timer : 1 channel • Watchdog timer : 1 channel	
Timer output		4 (8-bit PWM output capable: 2)	
Clock output		• 65.5 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.10 MHz, 4.19 MHz, 8.38 MHz (at 8.38-MHz operation with main system clock) • 32.768 kHz (at 32.768-kHz operation with subsystem clock)	
Buzzer output		1.02 kHz, 2.05 kHz, 4.10 kHz, 8.19 kHz (at 8.38-MHz operation with main system clock)	
Vectored source	Maskable	Internal : 18 External : 5	Internal : 19 External : 5
	Non-maskable	Internal : 1	
	Software	1	
Power supply voltage		V_{DD} = 2.7 to 5.5 V	
Operating ambient temperature		T_A = –40 to +85°C	
Package		• 64-pin plastic QFP (14 × 14 mm) • 64-pin plastic LQFP (12 × 12 mm)	

Note Pins are multiplexed. Select either of these interfaces.

CONTENTS

1. PIN CONFIGURATION (Top View)

- **64-pin plastic QFP (14 × 14 mm)**
  μPD78F0078GC-×××-AB8, 78F0078YGC-×××-AB8
- **64-pin plastic LQFP (12 × 12 mm)**
  μPD78F0078GK-×××-8A8, 78F0078YGK-×××-8A8



Note SDA0 and SCL0 are only provided on the μPD78F0078Y.

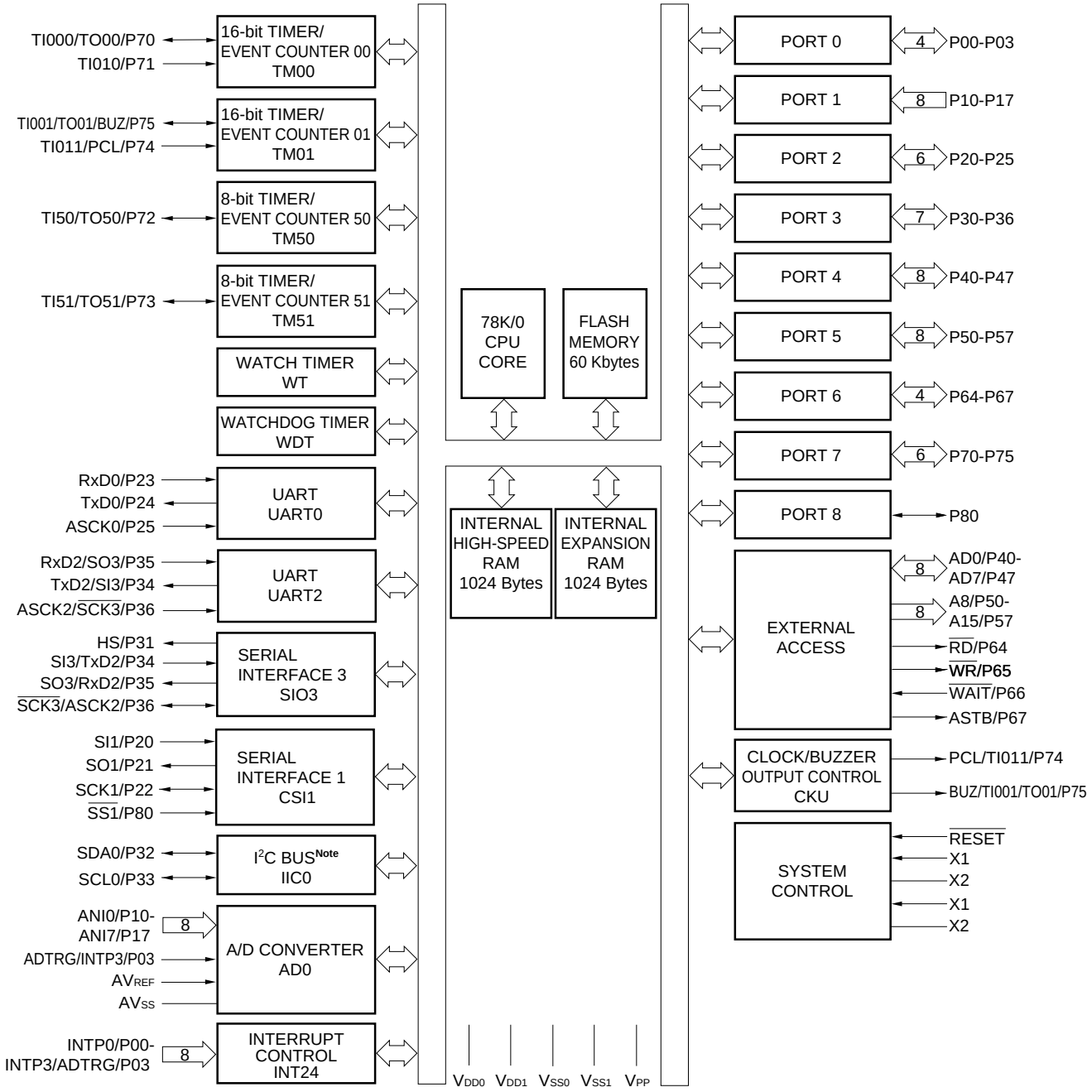
Cautions 1. Connect the V_{PP} pin directly to V_{SS0} or V_{SS1} in normal operation mode.

2. Connect the AV_{SS} pin to V_{SS0}.

Remark When used in applications where the noise generated inside the microcontroller needs to be reduced, the implementation of noise reduction measures, such as supplying voltage to V_{DD0} and V_{DD1} individually and connecting V_{SS0} and V_{SS1} to different ground lines, is recommended.

A8 to A15	: Address Bus	PCL	: Programmable Clock
AD0 to AD7	: Address/Data Bus	$\overline{RD}$	: Read Strobe
ADTRG	: AD Trigger Input	$\overline{RESET}$	: Reset
ANI0 to ANI7	: Analog Input	RxD0, RxD2	: Receive Data
ASCK0, ASCK2	: Asynchronous Serial Clock	SCK1, $\overline{SCK3}$, SCL0	: Serial Clock
ASTB	: Address Strobe	SDA0	: Serial Data
AV_{REF}	: Analog Reference Voltage	SI1, SI3	: Serial Input
AV_{SS}	: Analog Ground	SO1, SO3	: Serial Output
BUZ	: Buzzer Output	$\overline{SS1}$	: Serial Interface Chip Select Input
HS	: Hand Shake Output	TI000, TI010, TI001,	
INTP0 to INTP3	: External Interrupt Input	TI011, TI50, TI51	: Timer Input
P00 to P03	: Port 0	TO00, TO01, TO50, TO51	: Timer Output
P10 to P17	: Port 1	TxD0, TxD2	: Transmit Data
P20 to P25	: Port 2	V_{DD0}, V_{DD1}	: Power Supply
P30 to P36	: Port 3	V_{PP}	: Programming Power Supply
P40 to P47	: Port 4	V_{SS0}, V_{SS1}	: Ground
P50 to P57	: Port 5	$\overline{WAIT}$	: Wait
P64 to P67	: Port 6	$\overline{WR}$	: Write Strobe
P70 to P75	: Port 7	X1, X2	: Crystal (Main System Clock)
P80	: Port 8	XT1, XT2	: Crystal (Subsystem Clock)

2. BLOCK DIAGRAM



Note I^2C BUS is only provided on the μPD78F0078Y.

3. PIN FUNCTIONS

3.1 Port Pins (1/2)

Pin Name	I/O	Function		After Reset	Alternate Function
P00	I/O	Port 0 4-bit input/output port. Input/output can be specified bit-wise. An on-chip pull-up resistor can be connected by software.		Input	INTP0
P01					INTP1
P02					INTP2
P03					INTP3/ADTRG
P10 to P17	Input	Port 1 8-bit input only port.		Input	ANI0 to ANI7
P20	I/O	Port 2 6-bit input/output port. Input/output can be specified bit-wise. An on-chip pull-up resistor can be connected by software.		Input	SI1
P21					SO1
P22					SCK1
P23					RxD0
P24					TxD0
P25					ASCK0
P30	I/O	Port 3 7-bit input/output port. Input/output can be specified bit-wise.	N-ch open-drain input/output port. LEDs can be driven directly.	Input	—
P31					HS
P32					SDA0[Note]
P33					SCL0[Note]
P34			An on-chip pull-up resistor can be connected by software.		SI3/TxD2
P35					SO3/RxD2
P36					$\overline{\text{SCK3}}$/ASCK2
P40 to P47	I/O	Port 4 8-bit input/output port. Input/output can be specified bit-wise. An on-chip pull-up resistor can be connected by software. Interrupt request flag (KRIF) is set to 1 by the falling edge detection.		Input	AD0 to AD7
P50 to P57	I/O	Port 5 8-bit input/output port. LEDs can be driven directly. Input/output can be specified bit-wise. An on-chip pull-up resistor can be connected by software.		Input	A8 to A15
P64	I/O	Port 6 4-bit input/output port. Input/output can be specified bit-wise. An on-chip pull-up resistor can be connected by software.		Input	$\overline{\text{RD}}$
P65					$\overline{\text{WR}}$
P66					$\overline{\text{WAIT}}$
P67					ASTB

Note These pins are only provided on the μPD78F0078Y.

3.1 Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
P70	I/O	Port 7 6-bit input/output port. Input/output can be specified bit-wise. An on-chip pull-up resistor can be connected by software.	Input	TI000/TO00
P71				TI010
P72				TI50/TO50
P73				TI51/TO51
P74				TI011/PCL
P75				TI001/TO01/BUZ
P80	I/O	Port 8 1-bit input/output port. Input/output can be specified bit-wise. On-chip pull-up resistor can be connected by software.	Input	$\overline{SS1}$

3.2 Non-port Pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0-INTP2	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising edge and falling edge) can be specified.	Input	P00-P02
INTP3				P03/ADTRG
SI1	Input	Serial interface serial data input.	Input	P20
SI3				P34/TxD2
SO1	Output	Serial interface serial data output.	Input	P21
SO3				P35/RxD2
SDA0[Note]	I/O	Serial interface serial data input/output.	Input	P32
SCK1	I/O	Serial interface serial clock input/output.	Input	P22
$\overline{SCK3}$				P36/ASCK2
SCL0[Note]				P33
$\overline{SS1}$	Input	Serial interface chip select input.	Input	P80
RxD0	Input	Serial data input for asynchronous serial interface.	Input	P23
RxD2				P35/SO3
TxD0	Output	Serial data output for asynchronous serial interface.	Input	P24
TxD2				P34/SI3
ASCK0	Input	Serial clock input for asynchronous serial interface.	Input	P25
ASCK2				P36/$\overline{SCK3}$
TI000	Input	External count clock input to 16-bit timer (TM00). Capture trigger input to capture register (CR010) of 16-bit timer (TM00).	Input	P70/TO00
TI010		Capture trigger input to capture register (CR000) of 16-bit timer (TM00).		P71
TI001		External count clock input to 16-bit timer (TM01). Capture trigger input to capture register (CR011) of 16-bit timer (TM01).		P75/TO01/BUZ
TI011		Capture trigger input to capture register (CR001) of 16-bit timer (TM01).		P74/PCL
TI50		External count clock input to 8-bit timer (TM50).		P72/TO50
TI51		External count clock input to 8-bit timer (TM51).		P73/TO51

Note These pins are only provided on the μPD78F0078Y.

3.2 Non-port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
TO00	Output	16-bit timer (TM00) output.	Input	P70/TI000
TO01		16-bit timer (TM01) output.		P75/TI001/ BUZ
TO50		8-bit timer (TM50) output.		P72/TI50
TO51		8-bit timer (TM51) output.		P73/TI51
PCL	Output	Clock output (for trimming of main system clock and subsystem clock).	Input	P74/TI011
BUZ	Output	Buzzer output.	Input	P75/TI001/ TO01
AD0 to AD7	I/O	Lower address/data bus for extending memory externally.	Input	P40 to P47
A8 to A15	Output	Higher address bus for extending memory externally.	Input	P50 to P57
$\overline{RD}$	Output	Strobe signal output for read operation of external memory.	Input	P64
$\overline{WR}$		Strobe signal output for write operation of external memory.		P65
$\overline{WAIT}$	Input	Inserting wait for accessing external memory.	Input	P66
ASTB	Output	Strobe output which externally latches address information output to port 4 and port 5 to access external memory.	Input	P67
ANI0 to ANI7	Input	A/D converter analog input.	Input	P10 to P17
ADTRG	Input	A/D converter trigger signal input.	Input	P03/INTP3
HS	Output	Handshake output when writing data to the flash memory using SIO3.	Input	P31
AV_{REF}	Input	A/D converter reference voltage and analog power supply.	—	—
AV_{SS}	—	A/D converter ground potential. Set the same potential as that of V_{SS0} or V_{SS1}.	—	—
X1	Input	Connecting crystal resonator for main system clock oscillation.	—	—
X2	—		—	—
XT1	Input	Connecting crystal resonator for subsystem clock oscillation.	—	—
XT2	—		—	—
$\overline{RESET}$	Input	System reset input.	Input	—
V_{DD0}	—	Positive power supply for ports.	—	—
V_{DD1}	—	Positive power supply (except ports).	—	—
V_{SS0}	—	Ground potential of ports.	—	—
V_{SS1}	—	Ground potential (except ports).	—	—
V_{PP}	—	Applying high-voltage for program write/verify. Connect directly to V_{SS0} or V_{SS1} in normal operation mode.	—	—

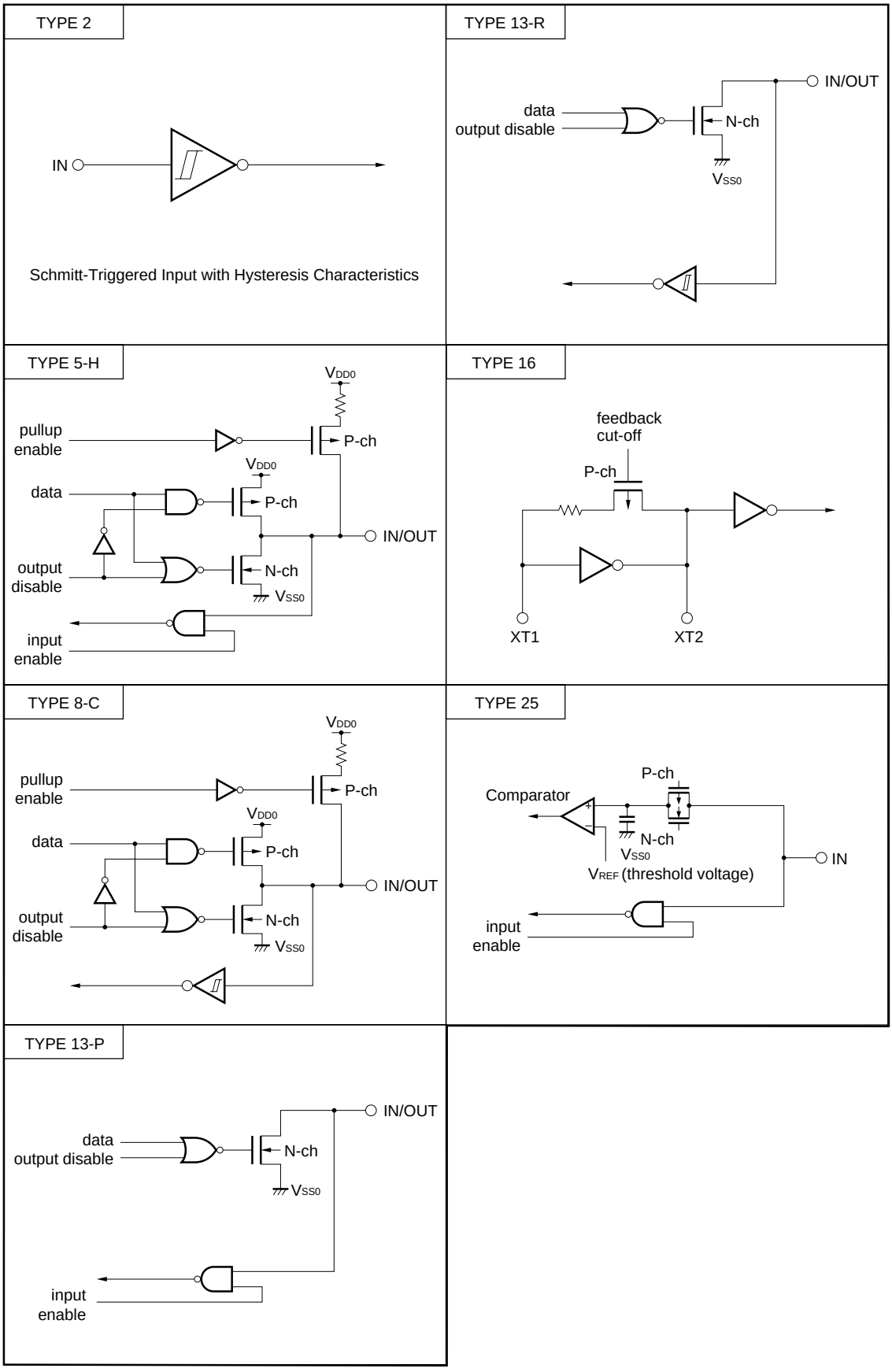
3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 3-1. For the input/output circuit configuration of each type, see Figure 3-1.

Table 3-1. Input/Output Circuit Type of Each Pin

Pin Name	Input/output Circuit Type	I/O	Recommended Connection When Not Used
P00/INTP0-P02/INTP2	8-C	Input/output	Independently connect to V_{SS0} via a resistor .
P03/INTP3/ADTRG			
P10/ANI0 to P17/ANI7	25	Input	Independently connect to V_{DD0} or V_{SS0} via a resistor.
P20/SI1	8-C	Input/output	
P21/SO1	5-H		
P22/SCK1	8-C		
P23/RxD0			
P24/TxD0	5-H		
P25/ASCK0	8-C		
P30	13-P		Independently connect to V_{DD0} via a resistor .
P31/HS			
P32, P33 (μPD78F0078 only)			
P32/SDA0 (μPD78F0078Y only)	13-R		
P33/SCL0 (μPD78F0078Y only)			
P34/SI3/TxD2	8-C		Independently connect to V_{DD0} or V_{SS0} via a resistor .
P35/SO3/RxD2			
P36/$\overline{SCK3}$/ASCK2			
P40/AD0 to P47/AD7	5-H		Independently connect to V_{DD0} via a resistor.
P50/A8 to P57/A15			Independently connect to V_{DD0} or V_{SS0} via a resistor.
P64/$\overline{RD}$			
P65/$\overline{WR}$			
P66/$\overline{WAIT}$			
P67/ASTB			
P70/TI000/TO00	8-C		
P71/TI010			
P72/TI50/TO50			
P73/TI51/TO51			
P74/TI011/PCL			
P75/TI001/TO01/BUZ			
P80/$\overline{SS1}$			Connect to V_{SS0} via a resistor.
$\overline{RESET}$	2	Input	—
XT1	16		Connect to V_{DD0}.
XT2		—	Leave open.
AV_{REF}	—		Connect to V_{DD0}.
AV_{SS}			Connect to V_{SS0}.
V_{PP}			Connect directly to V_{SS0} or V_{SS1}.

Figure 3-1. Pin Input/Output Circuits



4. DIFFERENCES BETWEEN μPD78F0078, 78F0078Y AND MASK ROM VERSION

The μPD78F0078 and 78F0078Y are products provided with a flash memory which enables on-board reading, erasing, and rewriting of programs with device mounted on target system.

Table 4-1 and 4-2 show the difference between the μPD78F0078, 78F0078Y and the mask ROM version.

Table 4-1. Difference between μPD78F0078 and Mask ROM Version

Item	μPD780076	μPD780078	μPD78F0078
Internal ROM capacity	48 Kbytes	60 Kbytes	60 Kbytes
Internal ROM structure	Mask ROM		Flash memory
Mask option to specify the on-chip pull-up resistors of pins P30 through P33	Possible		Not possible
IC pin	Provided		Not provided
V_{PP} and HS pins	Not provided		Provided
Electrical specifications	Refer to the data sheet of individual products.		

Table 4-2. Difference between μPD78F0078Y and Mask ROM Version

Item	μPD780076Y	μPD780078Y	μPD78F0078Y
Internal ROM capacity	48 Kbytes	60 Kbytes	60 Kbytes
Internal ROM structure	Mask ROM		Flash memory
Mask option to specify the on-chip pull-up resistors of pins P30 through P31	Possible		Not possible
IC pin	Provided		Not provided
V_{PP} and HS pins	Not provided		Provided
Electrical specifications	Refer to the data sheet of individual products.		

Caution The noise immunity and radiation differ between the PROM model and mask ROM model. To replace a PROM model with a mask ROM model in the course from experimental production to mass production, evaluate your system with the CS model (not ES model) of the mask ROM model.

5. MEMORY SIZE SWITCHING REGISTER (IMS)

This register sets a part of internal memory unused by software. The memory mapping can be made the same as that of mask ROM version with different type of internal memory (ROM, RAM).

The IMS is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets the IMS to CFH.

Figure 5-1. Format of Memory Size Switching Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	CFH	R/W

RAM2	RAM1	RAM0	Selection of Internal High-Speed RAM Capacity
1	1	0	1024 bytes
Others			Setting prohibited

ROM3	ROM2	ROM1	ROM0	Selection of Internal ROM Capacity
1	1	0	0	48 Kbytes
1	1	1	1	60 Kbytes
Others				Setting prohibited

Table 5-1 shows the IMS set value to make the memory mapping the same as that of mask ROM version.

Table 5-1. Set Value of Memory Size Switching Register

Target Mask ROM Version	IMS Set Value
μPD780076, 780076Y	CCH
μPD780078, 780078Y	CFH

6. INTERNAL EXPANSION RAM SIZE SWITCHING REGISTER (IXS)

This register sets the internal expansion RAM capacity.

The IXS is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets the IXS to 0CH.

Caution The default value of the IXS is 0CH (setting prohibited). Be sure to set 0AH at initial setting.

Figure 6-1. Format of Internal Expansion RAM Size Switching Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
IXS	0	0	0	IXRAM4	IXRAM3	IXRAM2	IXRAM1	IXRAM0	FFF4H	0CH	R/W

IXRAM4	IXRAM3	IXRAM2	IXRAM1	IXRAM0	Selection of Internal High-Speed RAM Capacity
0	1	0	1	0	1024 bytes
Others					Setting prohibited

7. FLASH MEMORY PROGRAMMING

Writing to a flash memory can be performed without removing the memory from the target system. Writing is performed connecting the dedicated flash programmer Flashpro II (part number: FL-PR2) and Flashpro III (part number: FL-PR3 and PG-FP3) to the host machine and the target system. Moreover, writing to flash memory can also be performed using a flash memory writing adapter connected to Flashpro II or Flashpro III.

Remark FL-PR2 and FL-PR3 are products of Naito Densei Machida Mfg. Co., Ltd.

7.1 Selection of Transmission Method

Writing to a flash memory is performed using Flashpro II or Flashpro III with a serial transmission mode. One of the transmission method is selected from those in Table 7-1. The selection of the transmission method is made by using the format shown in Figure 7-1. Each transmission method is selected by the number of V_{PP} pulses shown in Table 7-1.

Table 7-1. List of Transmission Method

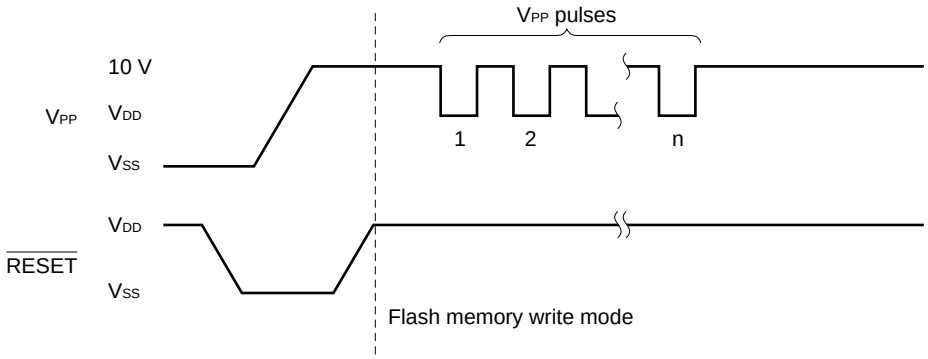
Transmission Method	Channels	Pin	V_{PP} Pulses
3-wire serial I/O (SIO3)	1	SI3/P34 SO3/P35 $\overline{SCK3}$/P36	1
		HS/P31 Note 1 SI3/P34 SO3/P35 SCK3/P36	3
I^2C bus (IIC0) Note 2	1	SDA0/P32 SCL0/P33	4
UART (UART0)	1	RxD0/P23 TxD0/P24	8

Notes 1. When using the handshake, use Flashpro III. Flashpro II cannot be used.

2. Provided on the μPD78F0078Y only.

Caution Select a transmission method always using the number of V_{PP} pulses shown in Table 7-1.

Figure 7-1. Format of Transmission Method Selection



7.2 Function of Flash Memory Programming

Operations such as writing to a flash memory are performed by various command/data transmission and reception operations according to the selected transmission method. Table 7-2 shows major functions of flash memory programming.

Table 7-2. Major Functions of Flash Memory Programming

Functions	Descriptions
Reset	Used to stop write operation and detect transmission cycle.
Batch verify	Compares the entire memory contents with the input data.
Batch delete	Deletes the entire memory contents.
Batch blank check	Checks the deletion status of the entire memory.
High-speed write	Performs write to the flash memory based on the write start address and the number of data to be written (number of bytes).
Continuous write	Performs continuous write based on the information input with high-speed write operation.
Status	Used to confirm the current operating mode and operation end.
Oscillation frequency setting	Sets the frequency of the resonator.
Delete time setting	Sets the memory delete time.
Silicon signature read	Outputs the device name and memory capacity, and device block information.

7.3 Connection of Flashpro II and Flashpro III

The connection of Flashpro II, Flashpro III and the μPD78F0078, 78F0078Y differs according to the transmission method (3-wire serial I/O[Note 1], UART, and I^2C bus[Note 2]). The connection for each transmission method is shown in Figures 7-2 through 7-5, respectively.

Notes 1. When using the handshake, use Flashpro III. Flashpro II cannot be used.

2. Provided on the μPD78F0078Y only.

Figure 7-2. Connection of Flashpro II and Flashpro III Using 3-Wire Serial I/O (SIO3) Method

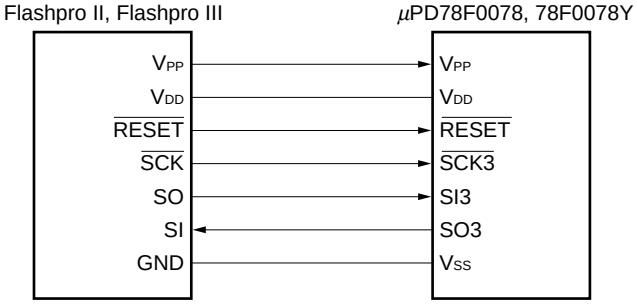


Figure 7-3. Connection of Flashpro III Using 3-Wire Serial I/O (SIO3) Method (When using handshake)

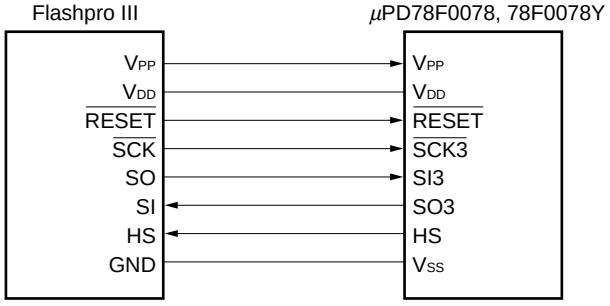


Figure 7-4. Connection of Flashpro II and Flashpro III Using I²C Bus (IIC0) Method (μPD78F0078Y only)

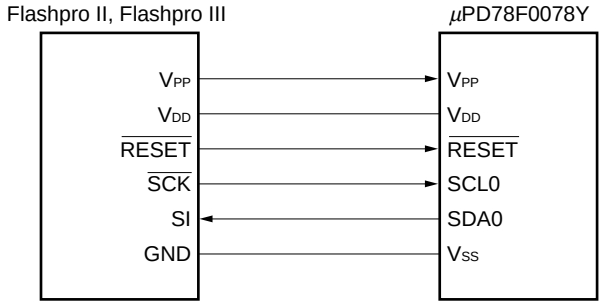
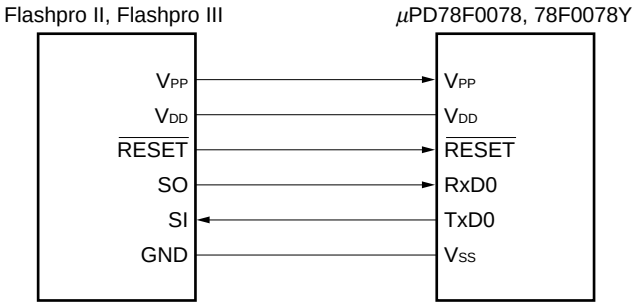


Figure 7-5. Connection of Flashpro II and Flashpro III Using UART (UART0) Method



8. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Test Conditions		Ratings	Unit
Supply voltage	V_{DD}			–0.3 to +6.5	V
	V_{PP}			–0.3 to +11.0	V
	AV_{REF}			–0.3 to V_{DD} + 0.3	V
	AV_{SS}			–0.3 to +0.3	V
Input voltage	V_{I1}	P00-P03, P10-P17, P20-P25, P34-P36, P40-P47, P50-P57, P64-P67, P70-P75, P80, X1, X2, XT1, XT2, $\overline{\text{RESET}}$		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P30-P33	N-ch open-drain	–0.3 to V_{DD} + 0.3	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	P10-P17	Analog input pin	AV_{SS} – 0.3 to AV_{REF} + 0.3 and –0.3 to V_{DD} + 0.3	V
High-level output current	I_{OH}	Per pin		–10	mA
		Total for P00-P03, P40-P47, P50-P57, P64-P67, P70-P75, P80		–15	mA
		Total for P20-P25, P30-P36		–15	mA
Low-level output current	I_{OL}	Per pin for P00-P03, P20-P25, P34-P36, P40-P47, P64-P67, P70-P75, P80		20	mA
		Per pin for P30-P33, P50-P57		30	mA
		Total for P00-P03, P40-P47, P64-P67, P70-P75, P80		50	mA
		Total for P20-P25		20	mA
		Total for P30-P36		100	mA
		Total for P50-P57		100	mA
Operating ambient tempature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

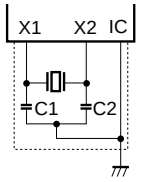
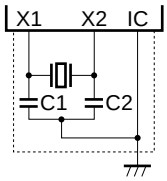
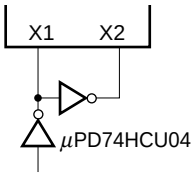
Caution Product quality may suffer if the absolute maximum rating is exceeded for even single parameter or even momentarily. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions ensuring that the absolute maximum ratings are not exceeded.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V.				15	pF
I/O capacitance	C_{IO}	f = 1 MHz Unmeasured pins returned to 0 V.	P00-P03, P20-P25, P34-P36, P40-P47, P50-P57, P64-P67, P70-P75, P80			15	pF
			P30-P33			20	pF

Remark Unless specified otherwise, alternate-function pin characteristics are the same as port pin characteristics.

Main System Clock Oscillator Characteristics (T_A = –40 to 85°C, V_{DD} = 2.7 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)**Note 1**	V_{DD} = 4.0 to 5.5 V	1.0		8.38	MHz
				1.0		5.0	MHz
		Oscillation stabilization time**Note 2**	After V_{DD} reaches oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequency (f_X)**Note 1**	V_{DD} = 4.0 to 5.5 V	1.0		8.38	MHz
				1.0		5.0	MHz
		Oscillation stabilization time**Note 2**	V_{DD} = 4.0 to 5.5 V			10	ms
						30	ms
External clock		X1 input frequency (f_X)**Note 1**	V_{DD} = 4.0 to 5.5 V	1.0		8.38	MHz
						5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})	V_{DD} = 4.0 to 5.5 V	50		500	ns
				85		500	ns

Notes 1. Indicates only oscillator characteristics.

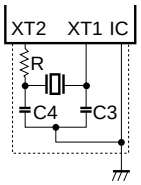
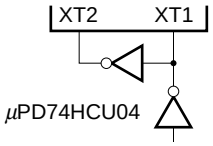
2. Time required to stabilize oscillation after reset or STOP mode release.

Cautions 1. When using the main system clock oscillator, wiring in the area enclosed with the broken line in the above figures should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a line through which a high fluctuating current flows.**
- **Always keep the ground point of the oscillator to the same potential as V_{SS1}.**
- **Do not ground the capacitor to a ground pattern in which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched again to the main system clock after the oscillation stabilization time is secured by the program.

Subsystem Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})**Note 1**		32	32.768	35	kHz
		Oscillation stabilization time**Note 2**	V_{DD} = 4.0 to 5.5 V		1.2	2	s
						10	s
External clock		XT1 input frequency (f_{XT})**Note 1**		32		38.5	kHz
		XT1 input high-/low- level width (t_{XTH}, t_{XTL})		5		15	μs

Notes 1. Indicates only oscillator characteristics.

2. Time required to stabilize oscillation after V_{DD} reaches oscillation voltage MIN.

Cautions 1. When using the subsystem clock oscillator, wiring in the area enclosed with the broken line in the above figures should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a line through which a high fluctuating current flows.**
- **Always keep the ground point of the oscillator to the same potential as V_{SS1}.**
- **Do not ground the capacitor to a ground pattern in which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subsystem clock oscillator is a low-amplitude circuit in order to achieve a low consumption current, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
High-level output current	I_{OH}	Per pin				–1	mA
		All pins				–20	mA
Low-level output current	I_{OL}	Per pin for P00-P03, P20-P25, P34-P36, P40-P47, P64-P67, P70-P75, P80				10	mA
		Per pin for P30-P33, P50-P57				15	mA
		Total for P00-P03, P40-P47, P64-P67, P70-P75, P80				20	mA
		Total for P20-P25				10	mA
		Total for P30-P36				70	mA
		Total for P50-P57				70	mA
High-level input voltage	V_{IH1}	P10-P17, P21, P24, P35, P40-P47, P50-P57, P64-P67, P74, P75		0.7 V_{DD}		V_{DD}	V
	V_{IH2}	P00-P03, P20, P22, P23, P25, P34, P36, P70-P73, P80, $\overline{\text{RESET}}$		0.8 V_{DD}		V_{DD}	V
	V_{IH3}	P30-P33 (N-ch open-drain)		0.7 V_{DD}		V_{DD}	V
	V_{IH4}	X1, X2		V_{DD} – 0.5		V_{DD}	V
	V_{IH5}	XT1, XT2	V_{DD} = 4.0 to 5.5 V	0.8 V_{DD}		V_{DD}	V
Low-level input voltage	V_{IL1}	P10-P17, P21, P24, P35, P40-P47, P50-P57, P64-P67, P74, P75		0		0.3 V_{DD}	V
	V_{IL2}	P00-P03, P20, P22, P23, P25, P34, P36, P70-P73, P80, $\overline{\text{RESET}}$		0		0.2 V_{DD}	V
	V_{IL3}	P30-P33 (N-ch open-drain)	4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.3 V_{DD}	V
			2.7 V ≤ V_{DD} < 4.0 V	0		0.2 V_{DD}	V
	V_{IL4}	X1, X2		0		0.4	V
	V_{IL5}	XT1, XT2	V_{DD} = 4.0 to 5.5 V	0		0.2 V_{DD}	V
High-level output voltage	V_{OH1}	V_{DD} = 4.0 to 5.5 V, I_{OH} = –1mA		V_{DD} – 1.0		V_{DD}	V
		I_{OH} = –100 μA		V_{DD} – 0.5		V_{DD}	V
Low-level output voltage	V_{OL1}	P30-P33, P50-P57	V_{DD} = 4.0 to 5.5 V, I_{OL} = 15 mA		0.4	2.0	V
		P00-P03, P20-P25, P34-P36, P40-P47, P64-P67, P70-P75, P80	V_{DD} = 4.0 to 5.5 V, I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	I_{OL} = 400 μA				0.5	V

Remark Unless specified otherwise, alternate-function pin characteristics are the same as port pin characteristics.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
High-level input leakage current	I_{LIH1}	$V_{IN} = V_{DD}$	P00-P03, P10-P17, P20-P25, P34-P36, P40-P47, P50-P57, P60-P67, P70-P75, P80, $\overline{\text{RESET}}$			3	μA
	I_{LIH2}		X1, X2, XT1, XT2			20	μA
	I_{LIH3}	V_{IN} = 5.5 V	P30 to P33			3	μA
Low-level input leakage current	I_{LIL1}	V_{IN} = 0 V	P00-P03, P10-P17, P20-P25, P34-P36, P40-P47, P50-P57, P64-P67, P70-P75, P80, $\overline{\text{RESET}}$			–3	μA
	I_{LIL2}		X1, X2, XT1, XT2			–20	μA
	I_{LIL3}		P30-P33			–3	μA
High-level output leakage current	I_{LOH}	$V_{OUT} = V_{DD}$				3	μA
Low-level output leakage current	I_{LOL}	V_{OUT} = 0 V				–3	μA
Software pull-up resistor	R_2	V_{IN} = 0 V, P00-P03, P20-P25, P34-P36, P40-P47, P50-P57, P64-P67, P70-P75, P80		15	30	90	kΩ

Remark Unless specified otherwise, alternate-function pin characteristics are the same as port pin characteristics.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions			MIN.	TYP.	MAX.	Unit
Power supply current[Note 1]	I_{DD1}[Note 2]	8.38-MHz crystal oscillation operating mode	V_{DD} = 5.0 V ± 10 %[Note 3]	When A/D converter stopped		10.5	21.0	mA
				When A/D converter is operating		11.5	23.0	mA
		5.0-MHz crystal oscillation operating	V_{DD} = 3.0 V ± 10 %[Note 3]	When A/D converter stopped		4.5	9.0	mA
				When A/D converter is operating		5.5	11.0	mA
	I_{DD2}	8.38-MHz crystal oscillation HALT mode	V_{DD} = 5.0 V ± 10 %[Note 3]	When peripheral function stopped		1.2	2.4	mA
				When peripheral function is operating			5	mA
		5.0-MHz crystal oscillation HALT mode	V_{DD} = 3.0 V ± 10 %[Note 3]	When peripheral function stopped		0.4	0.8	mA
				When peripheral function is operating			1.7	mA
	I_{DD3}	32.768-kHz crystal oscillation operating mode[Note 4]	V_{DD} = 5.0 V ± 10 %			115	230	μA
			V_{DD} = 3.0 V ± 10 %			95	190	μA
	I_{DD4}	32.768-kHz crystal oscillation HALT mode[Note 4]	V_{DD} = 5.0 V ± 10 %			15	45	μA
			V_{DD} = 3.0 V ± 10 %			5	15	μA
	I_{DD5}	STOP mode	V_{DD} = 5.0 V ± 10 %			0.1	30	μA
			V_{DD} = 3.0 V ± 10 %			0.05	10	μA

Notes 1. Total current flowing in the internal power supply (V_{DD1}).

2. Includes the peripheral operating current. However, the pull-up resistor on the port and the current flowing in the AV_{REF} pin are not included.

3. When the processor clock control register (PCC) is set to 00H.

4. When the main system clock has been stopped.

AC Characteristics

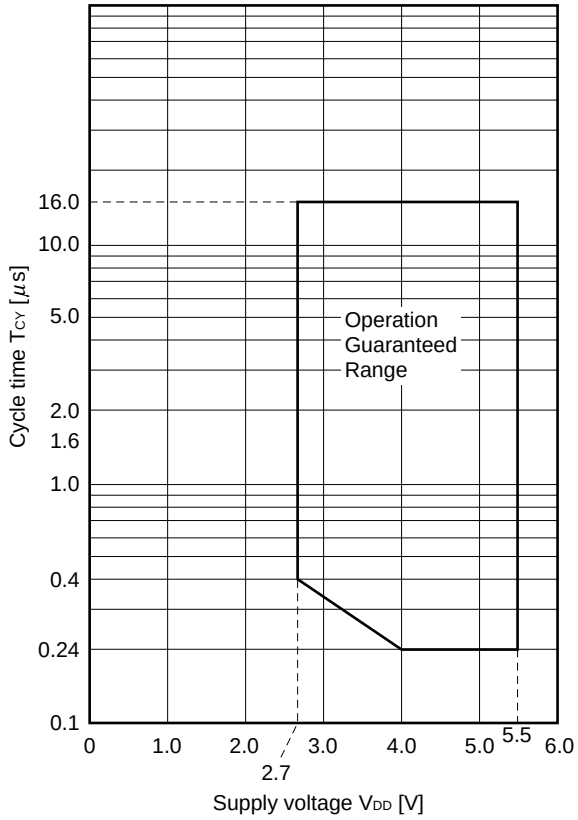
(1) Basic Operation (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (Min. instruction execution time)	T_{CY}	Operating with main system clock	4.0 V ≤ V_{DD} ≤ 5.5 V	0.24		16	μs
			2.7 V ≤ V_{DD} < 4.0 V	0.4		16	μs
		Operating with subsystem clock		103.9 Note 1	122	125	μs
TI000, TI010, TI001, TI011 input high-/low-level width	t_{TIH0} t_{TIL0}	3.5 V ≤ V_{DD} ≤ 5.5 V		$2/f_{sam}$ + 0.1 Note2			μs
		2.7 V ≤ V_{DD} < 3.5 V		$2/f_{sam}$ + 0.2 Note2			μs
TI50, TI51 input frequency	f_{TI5}			0		4	MHz
TI50, TI51 input high-/low-level width	t_{TIH5} t_{TIL5}			100			ns
Interrupt request input high-/low-level width	t_{INTH} t_{INTL}	INTP0-INTP3, P40-P47		1			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			μs

Notes 1. Value when using the external clock. When using a crystal resonator, the value becomes 114 μs (MIN.).

2. Selection of f_{sam} = f_X, f_X/4, f_X/64 is available with bits 0 and 1 (PRM0n0, PRM0n1) of prescaler mode register 0n (PRM0n). However, if the TI00n valid edge is selected as the count clock, the value becomes f_{sam} = f_X/8 (n = 0, 1).

T_{CY} vs V_{DD} (at main system clock operation)



(2) Read/Write Operation (T_A = –40 to + 85°C, V_{DD} = 4.0 to 5.5 V) (1/2)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.3t_{CY}$		ns
Address setup time	t_{ADS}		20		ns
Address hold time	t_{ADH}		6		ns
Data input time from address	t_{ADD1}			$(2 + 2n)t_{CY}$ – 54	ns
	t_{ADD2}			$(3 + 2n)t_{CY}$ – 60	ns
Address output time from $\overline{RD}\downarrow$	t_{RDAD}		0	100	ns
Data input time from $\overline{RD}\downarrow$	t_{RDD1}			$(2 + 2n)t_{CY}$ – 87	ns
	t_{RDD2}			$(3 + 2n)t_{CY}$ – 93	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		$(1.5 + 2n)t_{CY}$ – 33		ns
	t_{RDL2}		$(2.5 + 2n)t_{CY}$ – 33		ns
$\overline{WAIT}\downarrow$ input time from $\overline{RD}\downarrow$	t_{RDWT1}			$0.5t_{CY}$ – 43	ns
	t_{RDWT2}			t_{CY} – 43	ns
$\overline{WAIT}\downarrow$ input time from $\overline{WR}\downarrow$	t_{WRWT}			$0.5t_{CY}$ – 25	ns
$\overline{WAIT}$ low-level width	t_{WTL}		$(0.5 + 2n)t_{CY}$ + 10	$(2 + 2n)t_{CY}$	ns
Write data setup time	t_{WDS}		60		ns
Write data hold time	t_{WDH}		6		ns
$\overline{WR}$ low-level width	t_{WRL1}		$(1.5 + 2n)t_{CY}$ – 15		ns
$\overline{RD}\downarrow$ delay time from ASTB$\downarrow$	t_{ASTRD}		6		ns
$\overline{WR}\downarrow$ delay time from ASTB$\downarrow$	t_{ASTWR}		$2t_{CY}$ – 15		ns
ASTB$\uparrow$ delay time from $\overline{RD}\uparrow$ in external fetch	t_{RDAST}		$0.8t_{CY}$ – 15	$1.2t_{CY}$	ns
Address hold time from $\overline{RD}\uparrow$ in external fetch	t_{RDADH}		$0.8t_{CY}$ – 15	$1.2t_{CY}$ + 30	ns
Write data output time from $\overline{RD}\uparrow$	t_{RDWD}		40		ns
Write data output time from $\overline{WR}\downarrow$	t_{WRWD}		10	60	ns
Address hold time from $\overline{WR}\uparrow$	t_{WRADH}		$0.8t_{CY}$ – 15	$1.2t_{CY}$ + 30	ns
$\overline{RD}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTRD}		$0.8t_{CY}$	$2.5t_{CY}$ + 25	ns
$\overline{WR}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTWR}		$0.8t_{CY}$	$2.5t_{CY}$ + 25	ns

Remarks 1. $t_{CY} = T_{CY}/4$

2. n indicates the number of waits.

3. C_L = 100 pF (C_L is the load capacitance of AD0 to AD7, A8 to A15, $\overline{RD}$, $\overline{WR}$, $\overline{WAIT}$, and ASTB pins)

(2) Read/Write Operation (T_A = –40 to + 85°C, V_{DD} = 2.7 to 4.0 V) (2/2)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.3t_{CY}$		ns
Address setup time	t_{ADS}		30		ns
Address hold time	t_{ADH}		10		ns
Data input time from address	t_{ADD1}			$(2 + 2n)t_{CY}$ – 108	ns
	t_{ADD2}			$(3 + 2n)t_{CY}$ – 120	ns
Address output time from $\overline{RD}\downarrow$	t_{RDAD}		0	200	ns
Data input time from $\overline{RD}\downarrow$	t_{RDD1}			$(2 + 2n)t_{CY}$ – 148	ns
	t_{RDD2}			$(3 + 2n)t_{CY}$ – 162	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		$(1.5 + 2n)t_{CY}$ – 40		ns
	t_{RDL2}		$(2.5 + 2n)t_{CY}$ – 40		ns
$\overline{WAIT}\downarrow$ input time from $\overline{RD}\downarrow$	t_{RDWT1}			$0.5t_{CY}$ – 60	ns
	t_{RDWT2}			t_{CY} – 60	ns
$\overline{WAIT}\downarrow$ input time from $\overline{WR}\downarrow$	t_{WRWT}			$0.5t_{CY}$ – 50	ns
$\overline{WAIT}$ low-level width	t_{WTL}		$(0.5 + 2n)t_{CY}$ + 10	$(2 + 2n)t_{CY}$	ns
Write data setup time	t_{WDS}		60		ns
Write data hold time	t_{WDH}		10		ns
$\overline{WR}$ low-level width	t_{WRL}		$(1.5 + 2n)t_{CY}$ – 30		ns
$\overline{RD}\downarrow$ delay time from ASTB↓	t_{ASTRD}		10		ns
$\overline{WR}\downarrow$ delay time from ASTB↓	t_{ASTWR}		$2t_{CY}$ – 30		ns
ASTB↑ delay time from $\overline{RD}\uparrow$ in external fetch	t_{RDAST}		$0.8t_{CY}$ – 30	$1.2t_{CY}$	ns
Address hold time from $\overline{RD}\uparrow$ in external fetch	t_{RDADH}		$0.8t_{CY}$ – 30	$1.2t_{CY}$ + 60	ns
Write data output time from $\overline{RD}\uparrow$	t_{RDWD}		40		ns
Write data output time from $\overline{WR}\downarrow$	t_{WRWD}		20	120	ns
Address hold time from $\overline{WR}\uparrow$	t_{WRADH}		$0.8t_{CY}$ – 30	$1.2t_{CY}$ + 60	ns
$\overline{RD}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTRD}		$0.5t_{CY}$	$2.5t_{CY}$ + 50	ns
$\overline{WR}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTWR}		$0.5t_{CY}$	$2.5t_{CY}$ + 50	ns

Remarks 1. $t_{CY} = T_{CY}/4$

2. n indicates the number of waits.

3. C_L = 100 pF (C_L is the load capacitance of AD0 to AD7, A8 to A15, $\overline{RD}$, $\overline{WR}$, $\overline{WAIT}$, and ASTB pins)

(3) Serial Interface (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

(a) SIO3 3-wire serial I/O mode ($\overline{SCK3}$ ... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK3}$ cycle time	t_{KCY1}	4.0 V ≤ V_{DD} ≤ 5.5 V	954			ns
		2.7 V ≤ V_{DD} < 4.0 V	1600			ns
$\overline{SCK3}$ high-/low-level width	t_{KH1}	4.0 V ≤ V_{DD} ≤ 5.5 V	$t_{KCY1}/2 – 50$			ns
	t_{KL1}	2.7 V ≤ V_{DD} < 4.0 V	$t_{KCY1}/2 – 100$			ns
SI3 setup time (to $\overline{SCK3}$↑)	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.0 V	150			ns
SI3 hold time (from $\overline{SCK3}$↑)	t_{KSI1}		400			ns
SO3 output delay time from $\overline{SCK3}$↓	t_{KSO1}	C = 100 pF**Note**			300	ns

Note C is the load capacitance of the $\overline{SCK3}$ and SO3 output lines.

(b) SIO3 3-wire serial I/O mode ($\overline{SCK3}$ ... External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK3}$ cycle time	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.0 V	1600			ns
$\overline{SCK3}$ high-/low-level width	t_{KH2}	4.0 V ≤ V_{DD} ≤ 5.5 V	400			ns
	t_{KL2}	2.7 V ≤ V_{DD} < 4.0 V	800			ns
SI3 setup time (to $\overline{SCK3}$↑)	t_{SIK2}		100			ns
SI3 hold time (from $\overline{SCK3}$↑)	t_{KSI2}		400			ns
SO3 output delay time from $\overline{SCK3}$↓	t_{KSO2}	C = 100 pF**Note**			300	ns

Note C is the load capacitance of the SO3 output line.

(c) CSI1 3-wire serial I/O mode (SCK1 ... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
SCK1 cycle time	t_{KCY3}	4.0 V ≤ V_{DD} ≤ 5.5 V	240			ns
		2.7 V ≤ V_{DD} < 4.0 V	T.B.D			ns
SCK1 high-/low-level width	t_{KH3}	4.0 V ≤ V_{DD} ≤ 5.5 V	t_{KCY3}/2–5			ns
	t_{KL3}	2.7 V ≤ V_{DD} < 4.0 V	T.B.D			ns
SI1 setup time (to SCK1↑)	t_{SIK3}		20			ns
SI1 hold time (to SCK1↑)	t_{KSI3}		110			ns
SO1 output delay time from SCK1↓	t_{KSO3}	C = 100 pF[Note]			150	ns

Note C is the load capacitance of the SCK1 and SO1 output lines.

(d) CSI1 3-wire serial I/O mode (SCK1 ... External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
SCK1 cycle time	t_{KCY4}	4.0 V ≤ V_{DD} ≤ 5.5 V	200			ns
		2.7 V ≤ V_{DD} < 4.0 V	T.B.D			ns
SCK1 high-/low-level width	t_{KH4}	4.0 V ≤ V_{DD} ≤ 5.5 V	90			ns
	t_{KL4}	2.7 V ≤ V_{DD} < 4.0 V	T.B.D			ns
SI1 setup time (to SCK1↑)	t_{SIK4}		20			ns
SI1 hold time (to SCK1↑)	t_{KSI4}		110			ns
SO1 output delay time from SCK1↓	t_{KSO4}	C = 100 pF[Note]			150	ns

Note C is the load capacitance of the SO1 output line.

(e) UART0 mode (Dedicated baud rate generator output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		4.0 V ≤ V_{DD} ≤ 5.5 V			125000	bps
		2.7 V ≤ V_{DD} < 4.0 V			78125	bps

(f) UART0 mode (External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
ASCK0 cycle time	t_{KCY5}	4.0 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.0 V	1600			ns
ASCK0 high-/low-level width	t_{KH5}	4.0 V ≤ V_{DD} ≤ 5.5 V	400			ns
	t_{KL5}	2.7 V ≤ V_{DD} < 4.0 V	800			ns
Transfer rate		4.0 V ≤ V_{DD} ≤ 5.5 V			39063	bps
		2.7 V ≤ V_{DD} < 4.0 V			19531	bps

(g) UART0 mode (Infrared data transfer mode)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Transfer rate		4.0 V ≤ V_{DD} ≤ 5.5 V		115200	bps
Bit rate allowable error		4.0 V ≤ V_{DD} ≤ 5.5 V		±0.87	%
Output pulse width		4.0 V ≤ V_{DD} ≤ 5.5 V	1.2	0.24/for[Note]	μs
Input pulse width		4.0 V ≤ V_{DD} ≤ 5.5 V	4/fx		μs

Note fbr: Specified baud rate

(h) UART2 (Dedicated baud rate generator output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		4.0 V ≤ V_{DD} ≤ 5.5 V			125000	bps
		2.7 V ≤ V_{DD} < 4.0 V			78125	bps

(i) UART2 (External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
ASCK2 cycle time	t_{KCY6}	4.0 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.0 V	1600			ns
ASCK2 high-/low-level width	t_{KH6}	4.0 V ≤ V_{DD} ≤ 5.5 V	400			ns
	t_{KL6}	2.7 V ≤ V_{DD} < 4.0 V	800			ns
Transfer rate		4.0 V ≤ V_{DD} ≤ 5.5 V			39063	bps
		2.7 V ≤ V_{DD} < 4.0 V			19531	bps

(j) UART2 (Infrared data transfer mode)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Transfer rate		4.0 V ≤ V_{DD} ≤ 5.5 V		115200	bps
Bit rate allowable error		4.0 V ≤ V_{DD} ≤ 5.5 V		±0.87	%
Output pulse width		4.0 V ≤ V_{DD} ≤ 5.5 V	1.2	0.24/fbr[Note]	μs
Input pulse width		4.0 V ≤ V_{DD} ≤ 5.5 V	4/f_X		μs

Note fbr: Specified baud rate

(k) I^2C bus mode

Parameter		Symbol	Standard Mode		High-speed Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCL0 clock frequency		f_{SCL}	0	100	0	400	kHz
Bus free time (between stop and start condition)		t_{BUF}	4.7	—	1.3	—	μs
Hold time[Note 1]		$t_{HD:STA}$	4.0	—	0.6	—	μs
SCL0 clock low-level width		t_{LOW}	4.7	—	1.3	—	μs
SCL0 clock high-level width		t_{HIGH}	4.0	—	0.6	—	μs
Start/restart condition setup time		$t_{SU:STA}$	4.7	—	0.6	—	μs
Data hold time	CBUS compatible master	$t_{HD:DAT}$	5.0	—	—	—	μs
	I^2C bus		0[Note 2]	—	0[Note 2]	0.9[Note 3]	μs
Data setup time		$t_{SU:DAT}$	250	—	100[Note 4]	—	ns
SDA0 and SCL0 signal rise time		t_R	—	1000	20 + 0.1Cb[Note 5]	300	ns
SDA0 and SCL0 signal fall time		t_F	—	300	20 + 0.1Cb[Note 5]	300	ns
Stop condition setup time		$t_{SU:STO}$	4.0	—	0.6	—	μs
Capacitive load per each bus line		Cb	—	400	—	400	pF
Spike pulse width controlled by input filter		t_{SP}	—	—	0	50	ns

Notes 1. On start condition, the first clock pulse is generated after hold period.

2. To fulfill undefined area of the SCL0 falling edge, it is necessary for the device to provide internally SDA0 signal (on $V_{IHmin.}$ of SCL0 signal) with at least 300 ns of hold time.

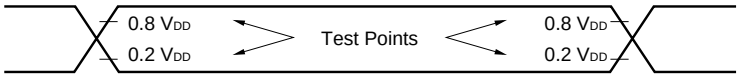
3. If the device does not extend the SCL0 signal low hold time (t_{LOW}), only maximum data hold time $t_{HD:DAT}$ needs to be fulfilled.

4. The high-speed mode I^2C bus is available in the standard mode I^2C bus system. At this time, the conditions described below must be satisfied.

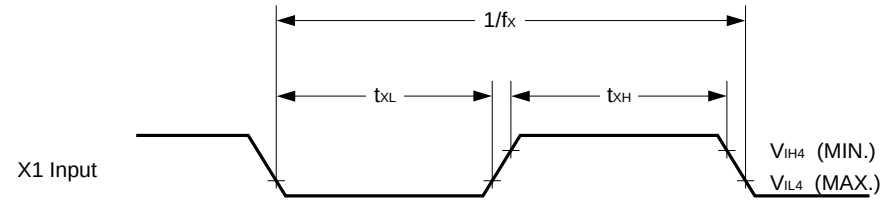
- If the device does not extend the SCL0 signal low state hold time
  $t_{SU:DAT} \geq 250$ ns
- If the device extends the SCL0 signal low state hold time
  Be sure to transmit the next data bit to the SDA0 line before the SCL0 line is released ($t_{Rmax.} + t_{SU:DAT}$ = 1000 + 250 = 1250 ns by standard mode I^2C bus specification).

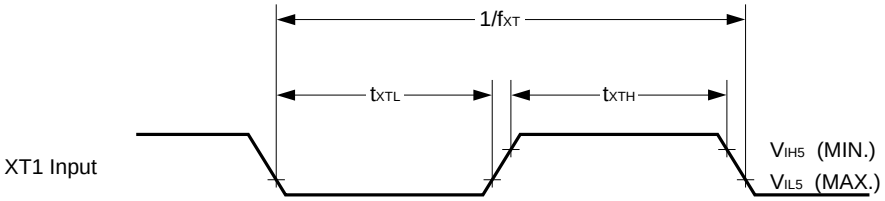
5. Cb : total capacitance per one bus line (unit : pF)

AC Timing Test Point (Excluding X1, XT1 Input)

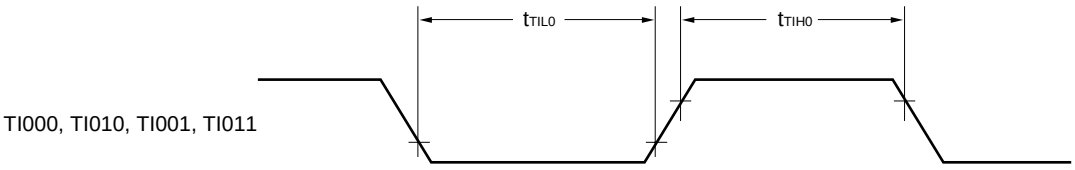


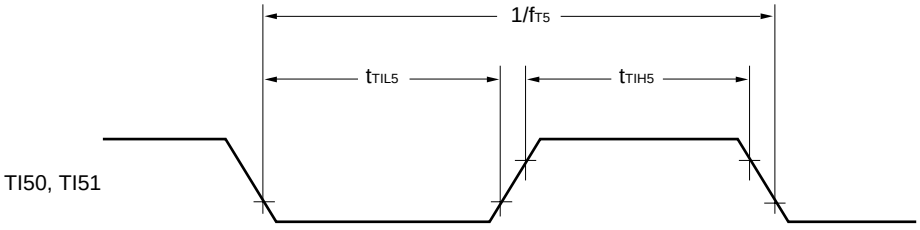
Clock Timing



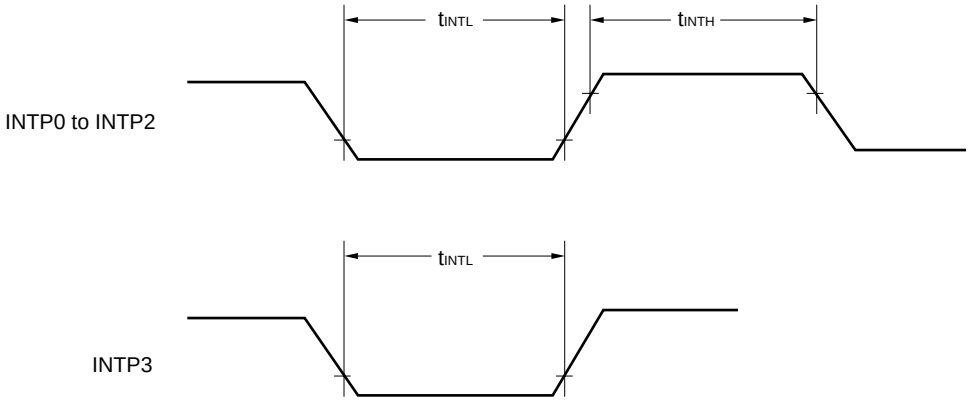


TI Timing

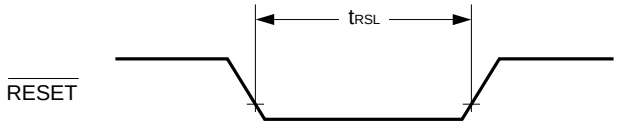




Interrupt Request Input Timing

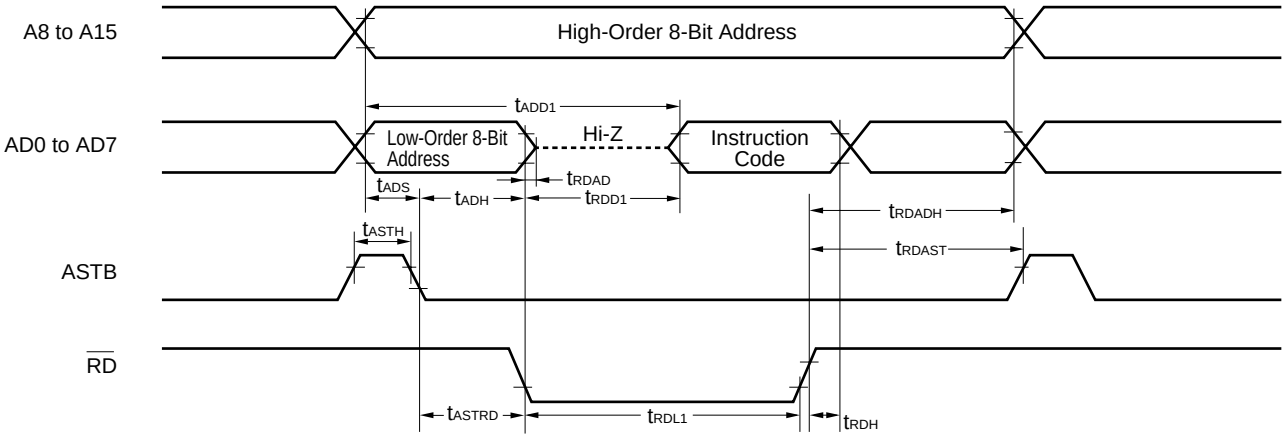


$\overline{\text{RESET}}$ Input Timing

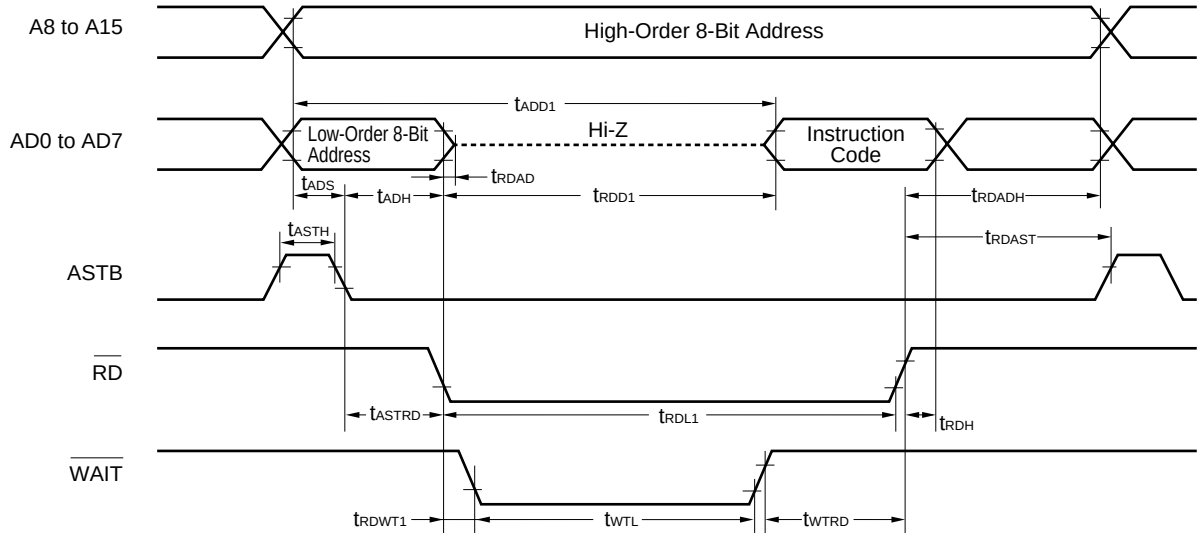


Read/Write Operation

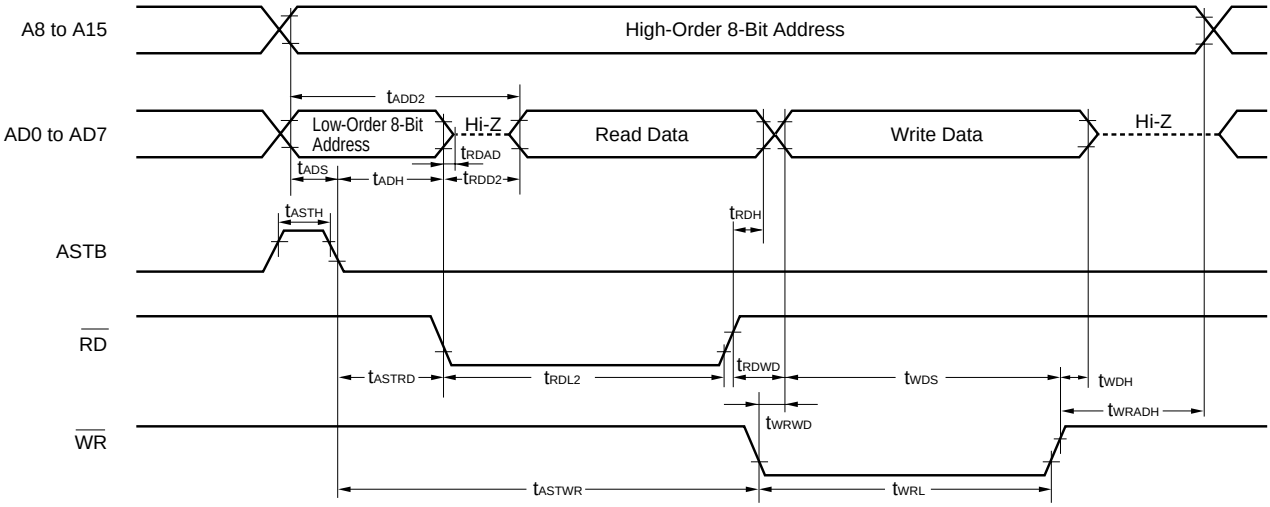
External Fetch (No Wait) :



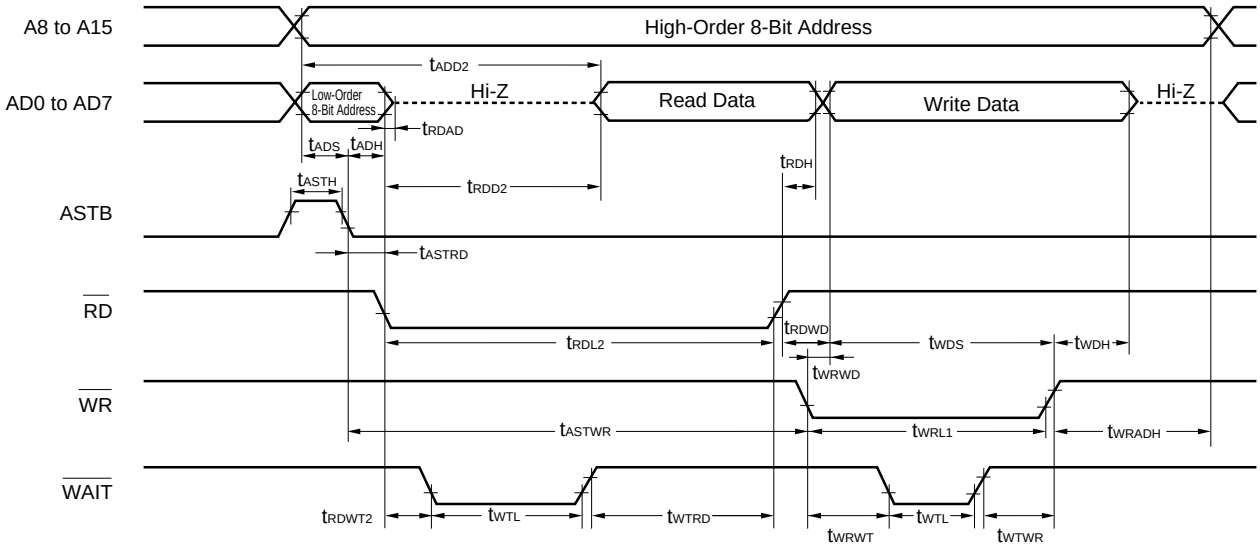
External Fetch (Wait Insertion) :



External Data Access (No Wait) :

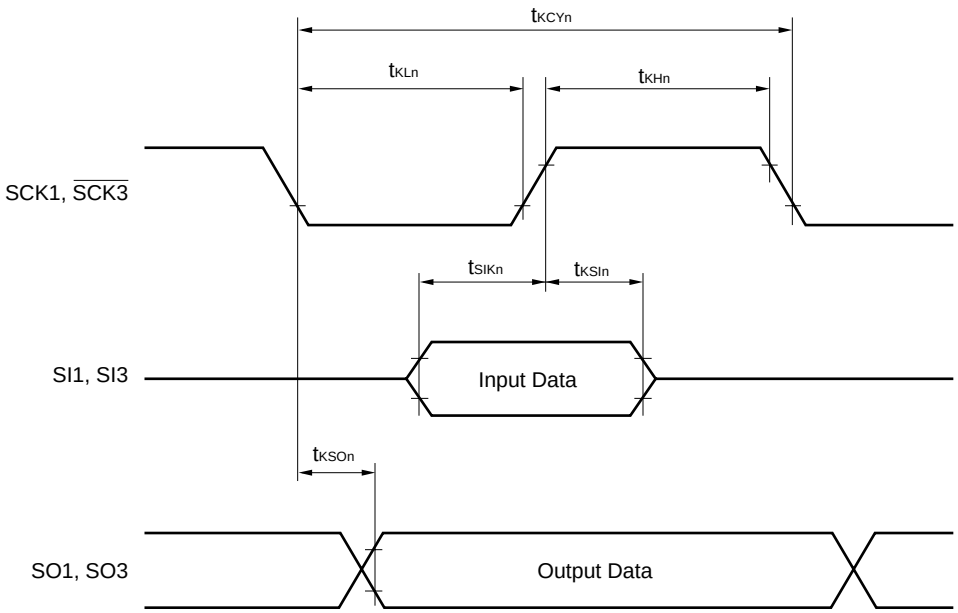


External Data Access (Wait Insertion) :



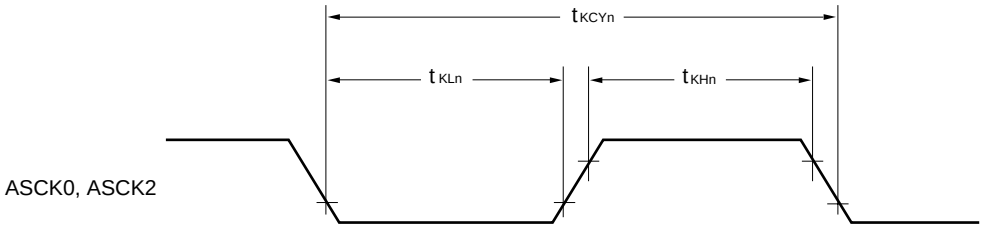
Serial Transfer Timing

3-wire Serial I/O Mode :



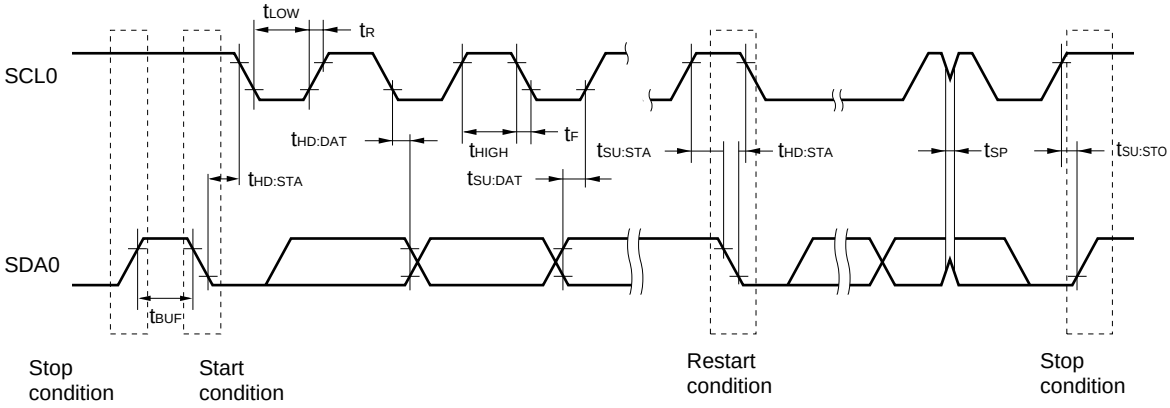
n = 1-4

UART Mode (External Clock Input) :



n = 5, 6

I²C Bus Mode



A/D Converter Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{REF} = 2.7 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	bit
Overall error[Note]		4.5 V ≤ AV_{REF} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.5 V			±0.7	%FSR
Conversion time	t_{CONV}	4.5 V ≤ AV_{REF} ≤ 5.5 V	14		144	μs
		2.7 V ≤ AV_{REF} < 4.5 V	19		144	μs
Analog input voltage	V_{IAN}		0		AV_{REF}+0.3	V
AV_{REF} resistance	R_{AIREF}		10	20		kΩ

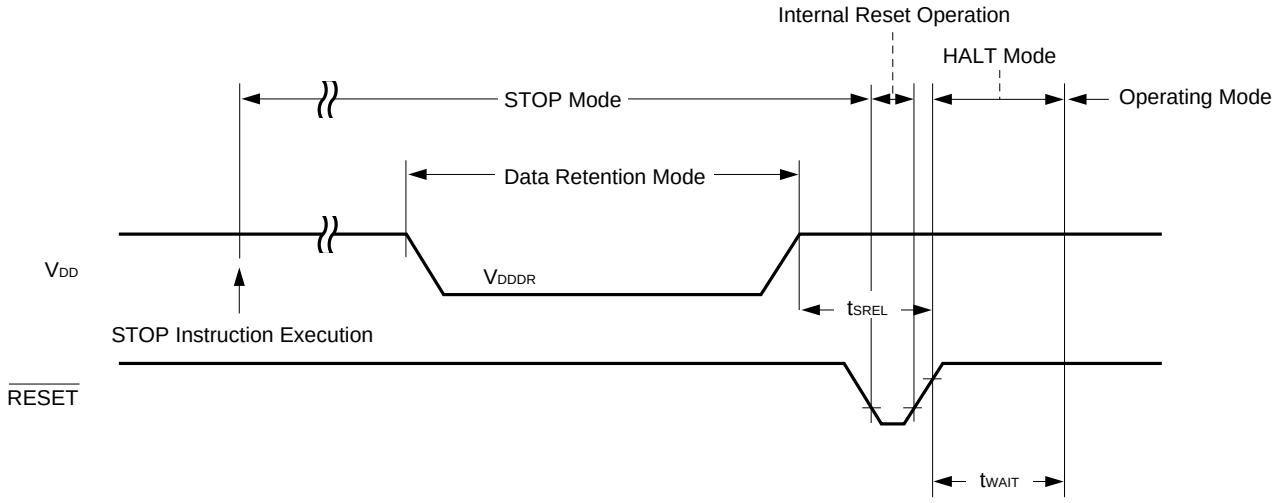
Note Overall error excluding quantization error (±1/2 LSB). It is indicated as a ratio to the full-scale value.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

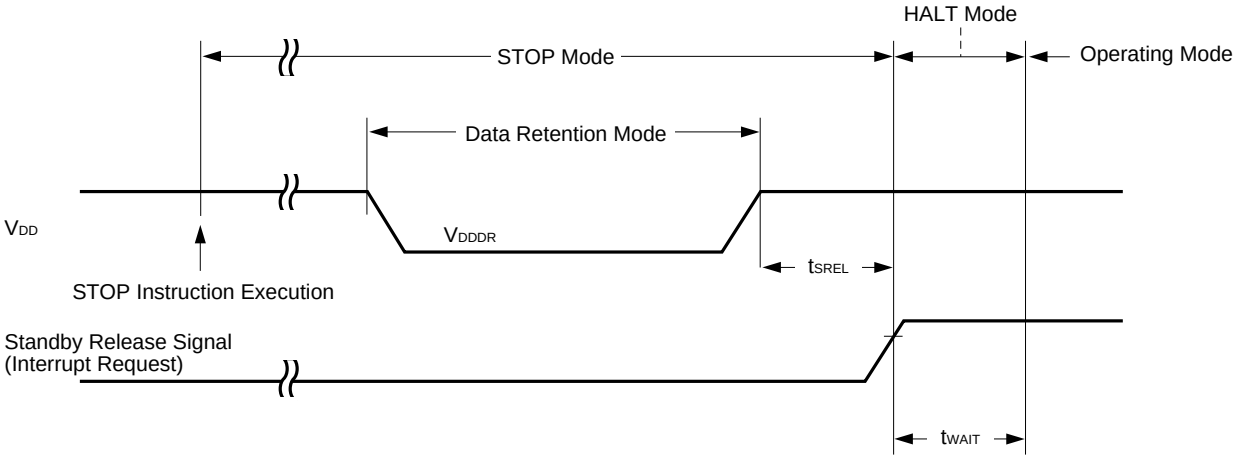
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		2.7		5.5	V
Data retention power supply current	I_{DDDR}	V_{DDDR} = 2.7 V		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{\text{RESET}}$		2^{17}/fx		ms
		Release by interrupt request		**Note**		ms

Note Selection of 2^{12}/fx and 2^{14}/fx to 2^{17}/fx is possible with bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).

Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)



Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Request Signal)



Flash Memory Programming Characteristics (V_{DD} = 2.7 to 5.5 V, V_{SS} = 0 V, V_{PP} = 9.7 to 10.3 V)

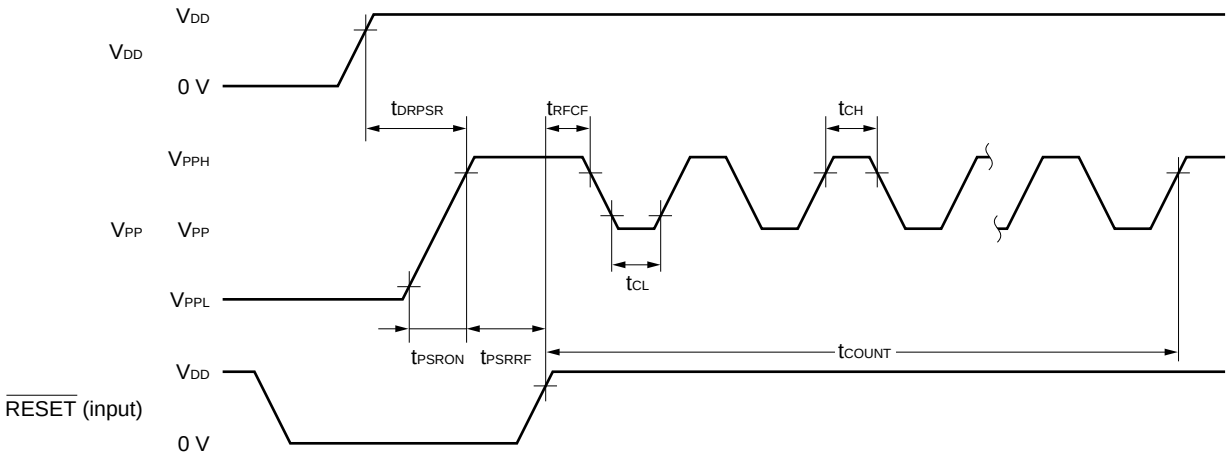
(1) Basic Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Operating frequency	f_X	4.0 V ≤ V_{DD} ≤ 5.5 V	10		8.38	MHz
		2.7 V ≤ V_{DD} ≤ 4.0 V	10		5.0	MHz
Supply voltage	V_{DD}	Operating voltage during write operation	2.7		5.5	V
	V_{PPL}	When detecting V_{PP} low level	0		0.2 V_{DD}	V
	V_{PP}	When detecting V_{PP} high level	0.8 V_{DD}	V_{DD}	1.2 V_{DD}	V
	V_{PPH}	When detecting V_{PP} high voltage	9.7	10.0	10.3	V
V_{DD} supply current	I_{DD}				10	mA
V_{PP} supply current	I_{PP}	V_{PP} = 10.0 V		75	100	mA
Write time (per byte)	T_{WRT}		50		500	μs
Write frequency	C_{WRT}				20	times
Erase time	T_{ERASE}		1		20	s
Programming temperature	T_{PRG}		0		+40	°C

(2) Write Operation Characteristics

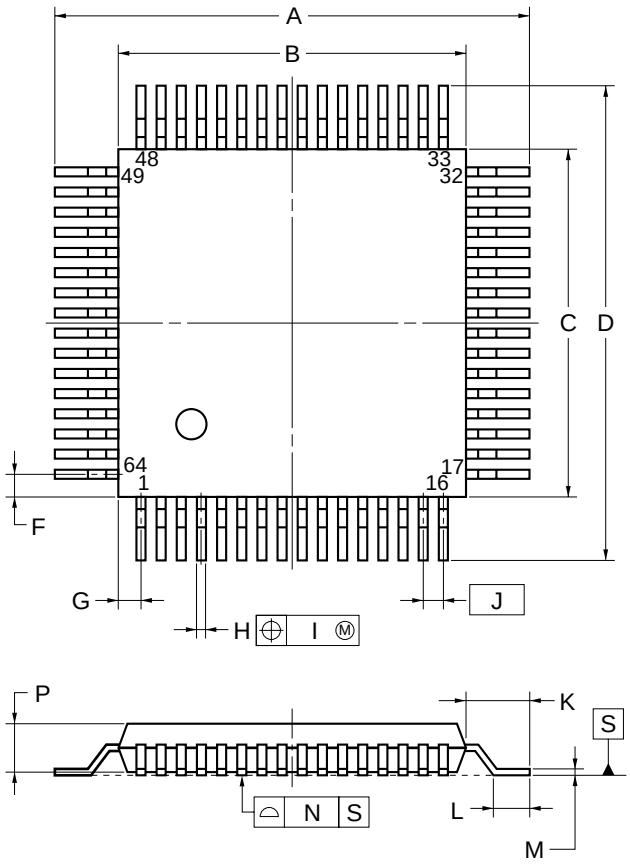
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
V_{PP} set time	t_{PSRON}	V_{PP} high voltage	1.0			μs
V_{PP}↑ set time from V_{DD}↑	t_{DRPSR}	V_{PP} high voltage	1.0			μs
$\overline{RESET}$↑ set time from V_{PP}↑	t_{PSRRF}	V_{PP} high voltage	1.0			μs
V_{PP} count start time from $\overline{RESET}$↑	t_{RFCF}		1.0			μs
Count execution time	t_{COUNT}				2.0	ms
V_{PP} counter high-/low-level width	t_{CH}, t_{CL}		8.0			μs
V_{PP} counter noise elimination width	t_{NFW}			40		ns

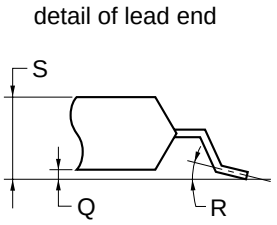
Flash Write Mode Setting Timing



9. PACKAGE DRAWINGS

64 PIN PLASTIC QFP (□14)





NOTE

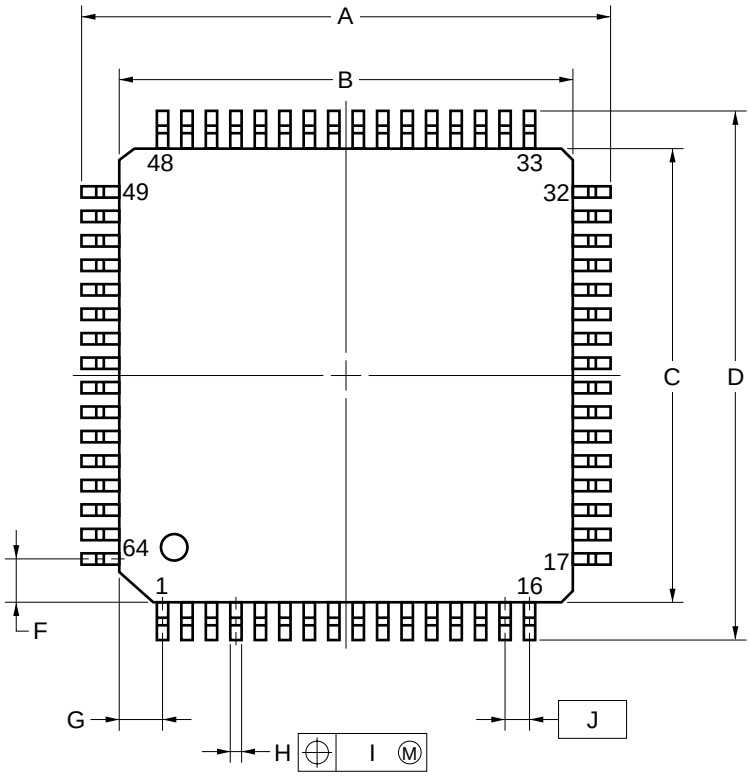
1. Controlling dimension —— millimeter.

2. Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

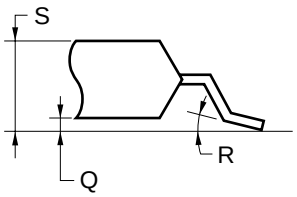
ITEM	MILLIMETERS	INCHES
A	17.6±0.4	0.693±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	$0.37^{+0.08}_{-0.07}$	$0.015^{+0.003}_{-0.004}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.17^{+0.08}_{-0.07}$	$0.007^{+0.003}_{-0.004}$
N	0.10	0.004
P	2.55±0.1	0.100±0.004
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	2.85 MAX.	0.113 MAX.

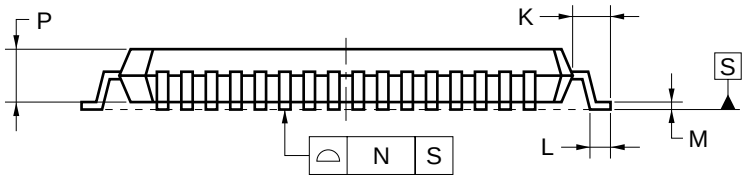
P64GC-80-AB8-4

64 PIN PLASTIC LQFP (12x12)



detail of lead end





NOTES

1. Controlling dimension — millimeter.

2. Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	14.8±0.4	0.583±0.016
B	12.0±0.2	$0.472^{+0.009}_{-0.008}$
C	12.0±0.2	$0.472^{+0.009}_{-0.008}$
D	14.8±0.4	0.583±0.016
F	1.125	0.044
G	1.125	0.044
H	0.32±0.08	$0.013^{+0.003}_{-0.004}$
I	0.13	0.005
J	0.65 (T.P.)	0.026
K	1.4±0.2	0.055±0.008
L	0.6±0.2	$0.024^{+0.008}_{-0.009}$
M	$0.17^{+0.08}_{-0.07}$	$0.007^{+0.003}_{-0.004}$
N	0.10	0.004
P	1.4±0.1	$0.055^{+0.004}_{-0.005}$
Q	0.125±0.075	0.005±0.003
R	5°±5°	5°±5°
S	1.7 MAX.	0.067 MAX.

P64GK-65-8A8-2

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD78F0078, 78F0078Y Subseries.

Also refer to **(5) Cautions on using development tools.**

(1) Language Processing Software

RA78K/0	Assembler package common to 78K/0 Series
CC78K/0	C compiler package common to 78K/0 Series
DF780078[Note]	Device file for μPD780078, 780078Y Subseries
CC78K/0-L	C compiler library source file common to 78K/0 Series

Note Under development

(2) Flash Memory Writing Tools

Flashpro II (FL-PR2) Flashpro III (FL-PR3, PG-FP3)	Flash programmer dedicated to on-chip flash memory microcontroller
FA-64GC FA-64GK	Adapter for flash memory writing • FA-64GC: For 64-pin plastic QFP (GC-AB8 type) • FA-64GK: For 64-pin plastic LQFP (GK-8A8 type)

(3) Debugging Tool

• When using in-circuit emulator IE-78K0-NS

IE-78K0-NS	In-circuit emulator common to 78K/0 Series
IE-70000-MC-PS-B	Power supply unit for IE-78K0-NS
IE-78K0-NS-PA[Note]	Performance board to enhance/expand functions of IE-78K0-NS
IE-70000-98-IF-C	Interface adapter when using PC-9800 series as host machine (excluding notebook PCs) (C bus compatible)
IE-70000-CD-IF-A	PC card and interface cable when using notebook PC as host machine (PCMCIA socket compatible)
IE-70000-PC-IF-C	Interface adapter when using IBM PC/AT™ compatible as host machine (ISA bus compatible)
IE-70000-PCI-IF	Adapter necessary when using on-chip PCI bus PC as host machine
IE-780034-NS-EM1	Emulation board common to μPD780034A Subseries
NP-64GC NP-64GC-TQ	Emulation probe for 64-pin plastic QFP (GC-AB8 type)
NP-64GK	Emulation probe for 64-pin plastic LQFP (GK-8A8 type)
EV-9200GC-64	Conversion socket for connecting target system designed to mount a 64-pin plastic QFP (GC-AB8 type) and NP-64GC
TGC-064SAP	Conversion adapter for connecting target system designed to mount a 64-pin plastic QFP (GC-AB8 type) and NP-64GC-TQ
TGK-064SBW	Conversion adapter for connecting target system board designed to mount a 64-pin plastic LQFP (GK-8A8 type) and NP-64GK
ID78K0-NS	Integrated debugger for IE-78K0-NS
SM78K0	System simulator common to 78K/0 Series
DF780078[Note]	Device file common to μPD780078, 780078Y Subseries

Note Under development

• **When using in-circuit emulator IE-78001-R-A**

IE-78001-R-A	In-circuit emulator common to 78K/0 Series
IE-70000-98-IF-C	Interface adapter when using PC-9800 series as host machine (excluding notebook PCs) (C bus compatible)
IE-70000-PC-IF-C	Interface adapter when using IBM PC/AT compatible as host machine (ISA bus compatible)
IE-70000-PCI-IF	Adapter necessary when using on-chip PCI bus PC as host machine
IE-78000-R-SV3	Interface adapter and cable when using EWS as host machine
IE-780034-NS-EM1	Emulation board common to μPD780034A Subseries
IE-78K0-R-EX1	Emulation probe conversion board necessary to use IE-780034-NS-EM1 on IE-78001-R-A
EP-78240GC-R	Emulation probe for 64-pin plastic QFP (GC-AB8 type)
EP-78012GK-R	Emulation probe for 64-pin plastic LQFP (GK-8A8 type)
EV-9200GC-64	Socket to be mounted on target system board manufactured for 64-pin plastic QFP (GC-AB8 type)
TGK-064SBW	Conversion adapter for connecting target system board designed to mount a 64-pin plastic LQFP (GK-8A8) and EP-78012GK-R.
ID78K0	Integrated debugger for IE-78001-R-A
SM78K0	System simulator common to 78K/0 Series
DF780078Note	Device file common to μPD780078, 780078Y Subseries

Note Under development

(4) Real-time OS

RX78K/0	Real-time OS for 78K/0 Series
MX78K0	OS for 78K/0 Series

(5) Cautions on using development tools

- The ID78K0-NS, ID78K0, and SM78K0 are used in combinaiton with the DF780078.
- The CC78K/0 and RX78K/0 are used in combination with the RA78K/0 and the DF780078.
- The FL-PR2, FL-PR3, FA-64GC, FA64GK, NP-64GC, NP-64GC-TQ, and NP-64GK are products made by Naito Densei Machida Mfg. Co., Ltd. (044-822-3813).
  Contact an NEC distributor when purchasing of these products.
- The TGC-064SAP and TGK-064SBW are products made by Tokyo Eletech Corp.
  Refer to: Daimaru Kogyo Ltd.
  Electronics Dept. (TEL: Tokyo 03-3820-7112)
  Electronics 2nd Dept. (TEL: Osaka 06-6244-6672)
- For third party development tools, see the **78K/0 Series Selection Guide (U11126E)**.
- The host machines and OSs supporting each software are as follows.

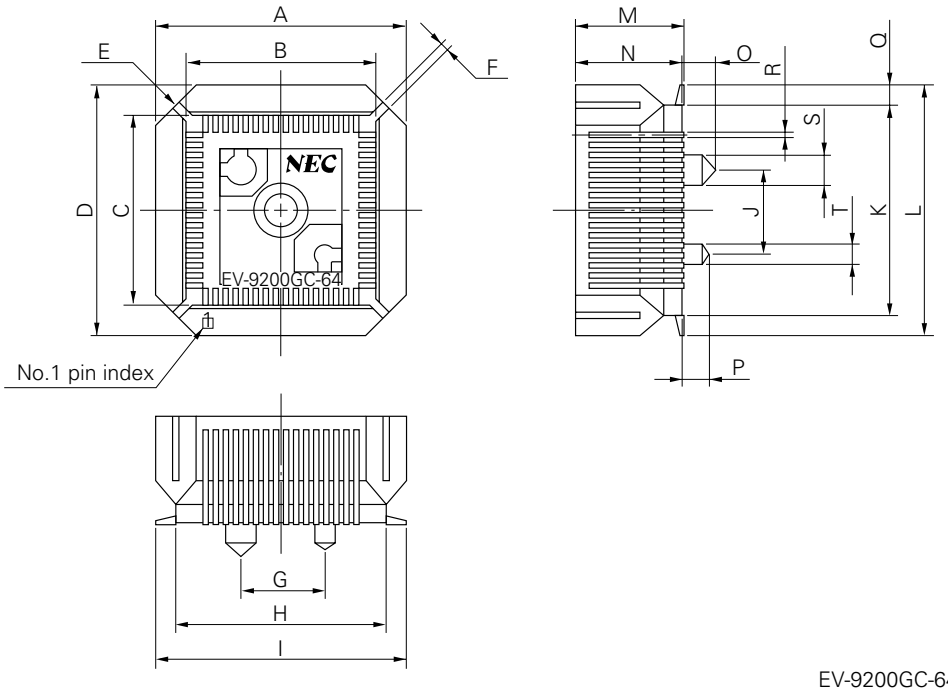
Host Machine / [OS] / Software	PC PC-9800 series [Windows™] IBM PC/AT compatible [Japanese/English Windows]	EWS HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™, Solaris™] NEWS™ (RISC) [NEWS-OS™]
RA78K/0	√ Note	√
CC78K/0	√ Note	√
ID78K0-NS	√	—
ID78K0	√	√
SM78K0	√	—
RX78K/0	√ Note	√
MX78K0	√ Note	√

Note DOS-based software

Conversion Socket (EV-9200GC-64) Package Drawing and Recommended Board Mounting Pattern

Figure A-1. EV-9200GC-64 Package Drawing (for reference)

Based on EV-9200GC-64
(1) Package drawing (in mm)

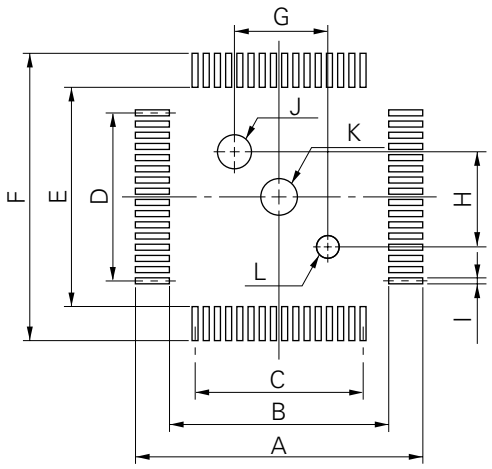


EV-9200GC-64-G0E

ITEM	MILLIMETERS	INCHES
A	18.8	0.74
B	14.1	0.555
C	14.1	0.555
D	18.8	0.74
E	4-C 3.0	4-C 0.118
F	0.8	0.031
G	6.0	0.236
H	15.8	0.622
I	18.5	0.728
J	6.0	0.236
K	15.8	0.622
L	18.5	0.728
M	8.0	0.315
N	7.8	0.307
O	2.5	0.098
P	2.0	0.079
Q	1.35	0.053
R	0.35±0.1	$0.014^{+0.004}_{-0.005}$
S	φ2.3	φ0.091
T	φ1.5	φ0.059

Figure A-2. EV-9200GC-64 Recommended Board Mounting Pattern (for reference)

Based on EV-9200GC-64
(2) Pad drawing (in mm)



EV-9200GC-64-P1E

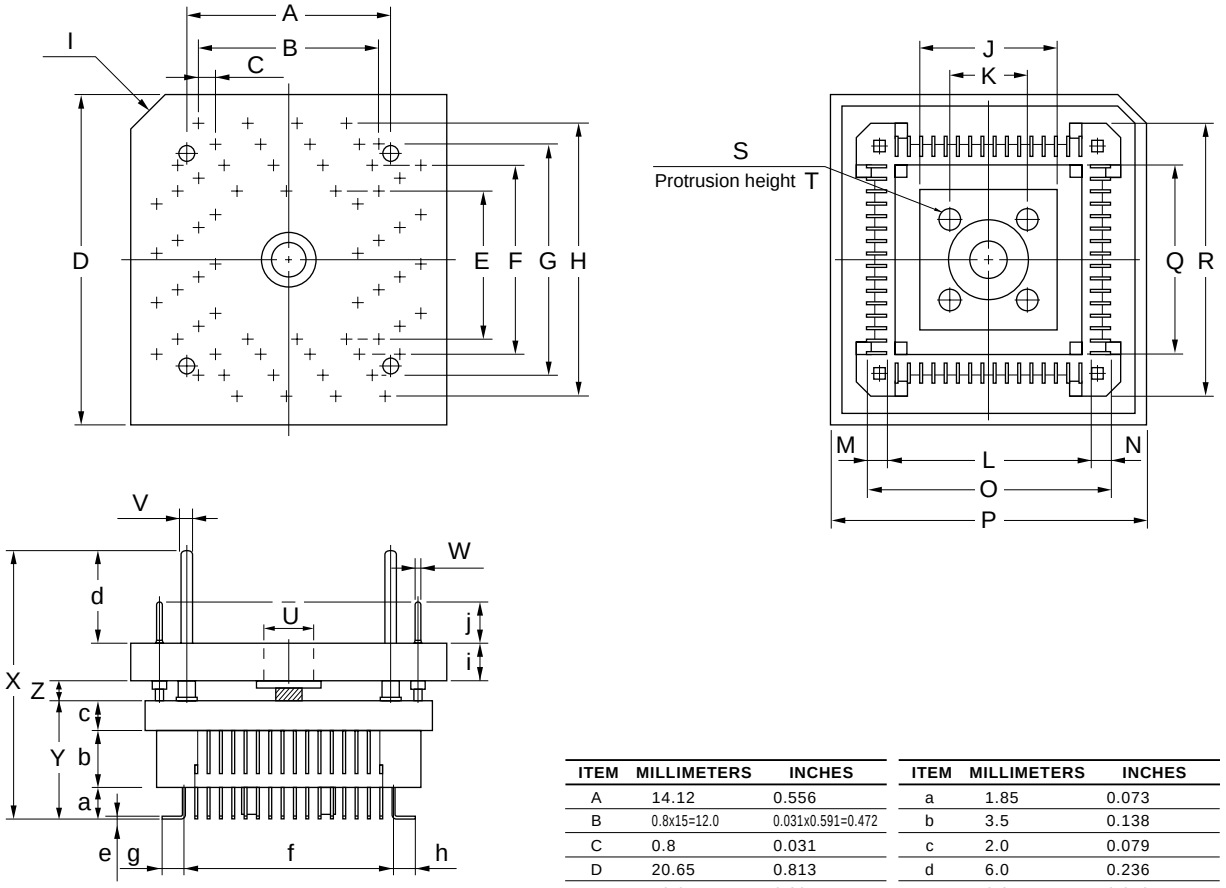
ITEM	MILLIMETERS	INCHES
A	19.5	0.768
B	14.8	0.583
C	$0.8\pm0.02\times15=12.0\pm0.05$	$0.031^{+0.002}_{-0.001}\times0.591=0.472^{+0.003}_{-0.002}$
D	$0.8\pm0.02\times15=12.0\pm0.05$	$0.031^{+0.002}_{-0.001}\times0.591=0.472^{+0.003}_{-0.002}$
E	14.8	0.583
F	19.5	0.768
G	6.00 ± 0.08	$0.236^{+0.004}_{-0.003}$
H	6.00 ± 0.08	$0.236^{+0.004}_{-0.003}$
I	0.5 ± 0.02	$0.197^{+0.001}_{-0.002}$
J	$\phi2.36\pm0.03$	$\phi0.093^{+0.001}_{-0.002}$
K	$\phi2.2\pm0.1$	$\phi0.087^{+0.004}_{-0.005}$
L	$\phi1.57\pm0.03$	$\phi0.062^{+0.001}_{-0.002}$

Caution Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E).

Conversion Adapter (TGC-064SAP) Package Drawing

Figure A-3. TGC-064SAP Package Drawing (for reference)

Reference diagram: TGC-064SAP (TQPACK064SA+TQSOCKET064SAP) Package dimension (unit: mm)



ITEM	MILLIMETERS	INCHES
A	14.12	0.556
B	0.8x15=12.0	0.031x0.591=0.472
C	0.8	0.031
D	20.65	0.813
E	10.0	0.394
F	12.4	0.488
G	14.8	0.583
H	17.2	0.677
I	C 2.0	C 0.079
J	9.05	0.356
K	5.0	0.197
L	13.35	0.526
M	1.325	0.052
N	1.325	0.052
O	16.0	0.630
P	20.65	0.813
Q	12.5	0.492
R	17.5	0.689
S	4-ϕ1.3	4-ϕ0.051
T	1.8	0.071
U	ϕ3.55	ϕ0.140
V	ϕ0.9	ϕ0.035
W	ϕ0.3	ϕ0.012
X	(19.65)	(0.667)
Y	7.35	0.289
Z	1.2	0.047

ITEM	MILLIMETERS	INCHES
a	1.85	0.073
b	3.5	0.138
c	2.0	0.079
d	6.0	0.236
e	0.25	0.010
f	13.6	0.535
g	1.2	0.047
h	1.2	0.047
i	2.4	0.094
j	2.7	0.106

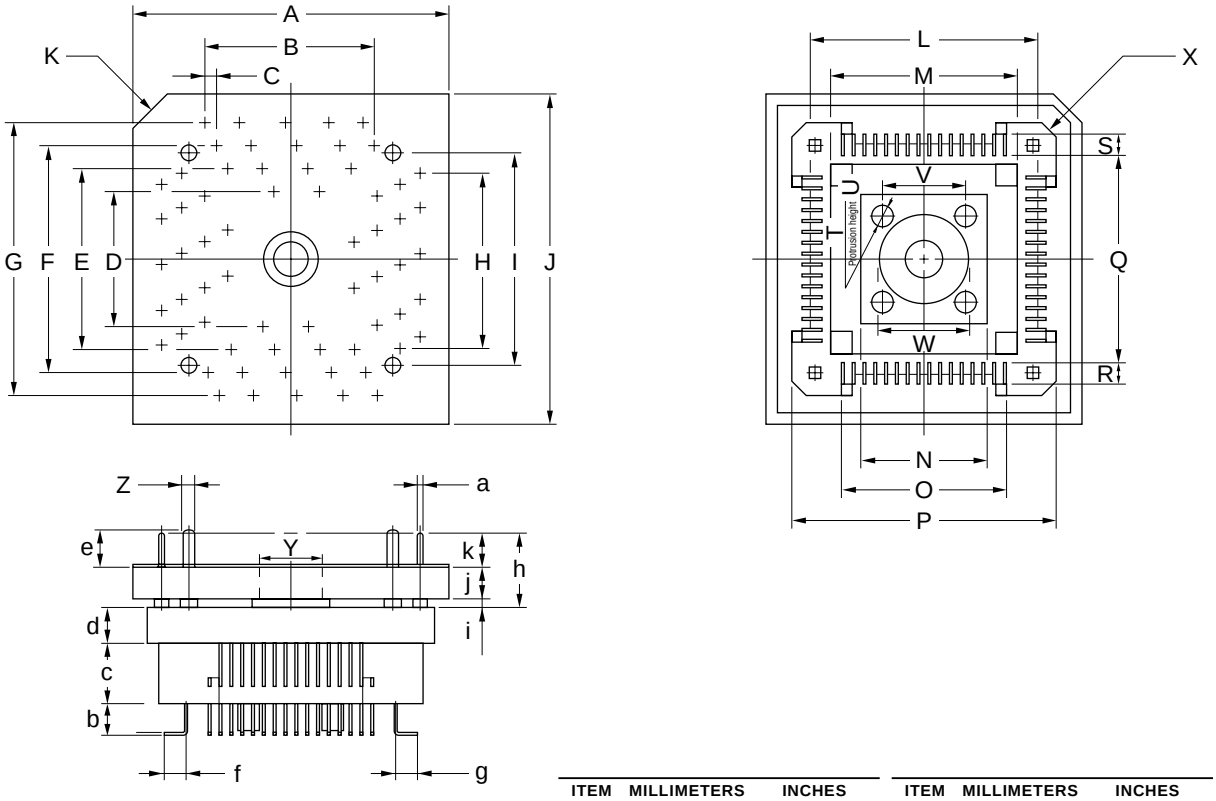
TGC-064SAP-G0E

note: Product by TOKYO ELETECH CORPORATION.

Conversion Adapter (TGK-064SBW) Package Drawing

Figure A-4. TGK-064SBW Package Drawing (for reference)

TGK-064SBW (TQPACK064SB + TQSOCKET064SBW) Package dimension (unit: mm)



ITEM	MILLIMETERS	INCHES
A	18.4	0.724
B	0.65x15=9.75	0.026x0.591=0.384
C	0.65	0.026
D	7.75	0.305
E	10.15	0.400
F	12.55	0.494
G	14.95	0.589
H	0.65x15=9.75	0.026x0.591=0.384
I	11.85	0.467
J	18.4	0.724
K	C 2.0	C 0.079
L	12.45	0.490
M	10.25	0.404
N	7.7	0.303
O	10.02	0.394
P	14.92	0.587
Q	11.1	0.437
R	1.45	0.057
S	1.45	0.057
T	4-ϕ1.3	4-ϕ0.051
U	1.8	0.071
V	5.0	0.197
W	ϕ5.3	ϕ0.209
X	4-C 1.0	4-C 0.039
Y	ϕ3.55	ϕ0.140
Z	ϕ0.9	ϕ0.035

ITEM	MILLIMETERS	INCHES
a	ϕ0.3	ϕ0.012
b	1.85	0.073
c	3.5	0.138
d	2.0	0.079
e	3.9	0.154
f	1.325	0.052
g	1.325	0.052
h	5.9	0.232
i	0.8	0.031
j	2.4	0.094
k	2.7	0.106

TGK-064SBW-G1E

note: Product by TOKYO ELETECH CORPORATION.

APPENDIX B. RELATED DOCUMENTS

Device-Related Documents

Document Name	Document No. (English)	Document No. (Japanese)
μPD780078, 780078Y Subseries User's Manual	To be prepared	U14260J (On preparation)
μPD780076, 780078, 780076Y, 780078Y Preliminary Product Information	U14259E	U14259J
μPD78F0078, 78F0078Y Preliminary Product Information	This document	U14258J
78K/0 Series User's Manual — Instructions	U12326E	U12326J

Development Tool Documents (User's Manual)

Document Name		Document No. (English)	Document No. (Japanese)
RA78K0 Assembler Package	Operation	U11802E	U11802J
	Language	U11801E	U11801J
	Structured Assembly Language	U11789E	U11789J
RA78K Series Structured Assembler Preprocessor		EEU-1402	U12323J
CC78K0 C Compiler	Operation	U11517E	U11517J
	Language	U11518E	U11518J
IE-78K0-NS		To be prepared	To be prepared
IE-78001-R-A		To be prepared	To be prepared
IE-78K0-R-EX1		To be prepared	To be prepared
IE-780034-NS-EM1		To be prepared	To be prepared
EP-78012GK-R		EEU-1538	EEU-5012
EP-78240		U10332E	EEU-986
SM78K0 System Simulator — Windows based	Reference	U10181E	U10181J
SM78K Series System Simulator	External Part User Open Interface Specifications	U10092E	U10092J
ID78K0-NS Integrated Debugger, Windows based	Reference	U12900E	U12900J
ID78K0 Integrated Debugger, EWS based	Reference	—	U11151J
ID78K0 Integrated Debugger, Windows based	Guide	U11649E	U11649J
ID78K0 Integrated Debugger, PC based	Reference	U11539E	U11539J

Caution The above related documents are subject to change without notice. Be sure to read the latest documents before designing.

Embedded Software Documents (User's Manual)

Document Name		Document No. (English)	Document No. (Japanese)
78K/0 Series Real-time OS	Fundamentals	U11537E	U11537J
	Installation	U11536E	U11536J
78K/0 Series OS MX78K0	Fundamental	U12257E	U12257J

Other Documents

Document Name	Document No. (English)	Document No. (Japanese)
SEMICONDUCTORS SELECTION GUIDE Products & Packages (CD-ROM)	X13769X	
Semiconductor Device Mounting Technology Manual	C10535E	C10535J
Quality Grades on NEC Semiconductor Devices	C11531E	C11531J
NEC Semiconductor Device Reliability/Quality Control System	C10983E	C10983J
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E	C11892J
Review of Quality and Reliability Handbook	–	C12769J
Guide to Microcomputer-Related Products by Third party	—	U11416J

Caution The above related documents are subject to change without notice. Be sure to read the latest documents before designing.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Purchase of NEC I^2C components conveys a license under the Philips I^2C Patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Philips.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

NEC Electronics Inc. (U.S.)
Santa Clara, California
Tel: 408-588-6000
800-366-9782
Fax: 408-588-6130
800-729-9288

NEC Electronics (Germany) GmbH
Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

NEC Electronics (UK) Ltd.
Milton Keynes, UK
Tel: 01908-691-133
Fax: 01908-670-290

NEC Electronics Italiana s.r.l.
Milano, Italy
Tel: 02-66 75 41
Fax: 02-66 75 42 99

NEC Electronics (Germany) GmbH
Benelux Office
Eindhoven, The Netherlands
Tel: 040-2445845
Fax: 040-2444580

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Tel: 08-63 80 820
Fax: 08-63 80 388

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Fax: 2886-9022/9044

NEC Electronics Hong Kong Ltd.
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Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

NEC Electronics Singapore Pte. Ltd.
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Tel: 65-253-8311
Fax: 65-250-3583

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  "Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.
  - Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
  - Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
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